

Department of Telecommunication

SEMESTER : 4th Sem M.Tech
BRANCH : TCE
SUBJECT : ECC
SUB CODE : 14ECS41
No of HRS/WK : 5

NAME OF THE FACULTY : Rahul Nyamangoudar
DATE OF COMMENCEMENT : 05/01/2016
DATE OF CLOSING : 11/04/2016
CLASS STRENGTH : 11
TOTAL HRS : 70

Session No	Chapter no (No of hrs planed for chapter)	Date	Topics planned for the session	Teaching Aids	Assignments / Tests planned for the chapter	Topics covered As per plan
1	1/0	5/1/2016	Basics of Digital Communication and Need of Coding?	Board, chalk, duster		
2	2/0	5/1/2016	Types of Codes, Modulation and Coding	„		
3	3/0	5/1/2016	Types of Errors, Maximum Likelihood decoding	„		
4	1/1	11/1/2016	Introduction to Algebra - Groups	„		
5	2/1	11/1/2016	Groups – Continued	„		
6	3/1	11/1/2016	Fields and Binary Field Arithmetic	„		
7	4/1	12/1/2016	Irreducible and Primitive Polynomials	„		
8	5/1	12/1/2016	Construction of Galois Field $GF(2^m)$	„		
9	6/1	12/1/2016	Basic Properties of Galois Field $GF(2^m)$	„		

10	7/1	18/1/2016	Minimal Polynomial, Computations using Galois Field $GF(2^m)$ Arithmetic.	Board, chalk, duster		
11	8/1	18/1/2016	Vector Spaces – subspace, span, Matrices – Generator and Parity Check	„		
12	9/1	18/1/2016	Road Map from Groups to Matrices and Previous QP Discussion.	„		
13	1/2	19/1/2016	Introduction to Linear Block Codes – Generator and Parity check Matrices	„		
14	2/2	19/1/2016	Encoding Circuit and Problem	„		
15	3/2	19/1/2016	Syndrome and Error Detection	„	Assignment 1	
16	4/2	25/1/2016	Minimum Distance of Block Code	„		
17	5/2	25/1/2016	Error detection and correction capabilities of linear block code	„		
18	6/2	25/1/2016	Standard Array and Syndrome Decoding	„		
19	7/2	1/2/2016	Hamming Codes	„		
20	8/2	1/2/2016	(24,12) Golay Code, Product Codes, Interleaved Codes	„		
21	9/2	1/2/2016	Reed Muller Codes – Construction	„		
22	10/2	2/2/2016	Reed Muller Codes Decoding	„		
23	11/2	2/2/2016	Reed Muller Codes Decoding – Contd	„		
24	12/2	2/2/2016	Reed Muller Codes Decoding – Contd. And Previous Year QP Discussion.	„		
25	1/3	8/2/2016	Cyclic Codes – Introduction and generator polynomial properties	„		
26	2/3	8/2/2016	Construction of Cyclic Codes	„		
27	3/3	8/2/2016	Generator and Parity Check Matrices and Encoding Circuit	Board, chalk, duster		
28	4/3	9/2/2016	Encoding Circuit using Parity Check Matrix	„		
29	5/3	9/2/2016	Syndrome Computation and Error Detection	„		
30	6/3	9/2/2016	Decoding of Cyclic Codes – Meggitt Decoder	„		

31	7/3	15/2/2016	Decoding of Cyclic Codes – With $r(x)$ shifted from right end	„		
32	8/3	15/2/2016	Cyclic Hamming Codes	„		
33	9/3	15/2/2016	Error Trapp Decoding	„		
34	10/3	16/2/2016	Improved Error Trap Decoding	„		
35	11/3	16/2/2016	(23,12) Golay Code	Board, chalk, duster		
36	12/3	16/2/2016	Shortened Cyclic Codes and Previous Year QP Discussion.	„	Assignment 2	
37	1/4	22/2/2016	Binary BCH Codes – Introduction, Construction and Generator Polynomial	„		
38	2/4	22/2/2016	Parity Check Matrix, Decoding of BCH Codes.	„		
39	3/4	22/2/2016	Iterative Algorithm for finding the error location polynomial	„		
40	4/4	23/2/2016	Implementation of Galois Field Arithmetic	„		
41	5/4	23/2/2016	Implementation of Galois Field Arithmetic (Contd.)	„		
42	6/4	23/2/2016	Implementation of Error Correction	„		
43	1/5	29/2/2016	Non-Binary BCH Codes – q-ARY Linear Block Codes	„		
44	2/5	29/2/2016	Primitive BCH Codes over $GF(q)$	„		
45	3/5	29/2/2016	Reed Solomon Codes	„		
46	4/5	1/3/2016	Decoding of Non-Binary BCH and RS Codes – Berlekamp Algorithm	„		
47	6/5	1/3/2016	Berlekamp Algorithm (Contd.)	„		
48	7/5	1/3/2016	Previous Year QP Discussion	„		
49	1/6	8/3/2016	Majority Logic decodable codes: One -step majority logic decoding	„		

50	2/6	8/3/2016	One -step majority logic decoding (Contd.)	Board, chalk, duster		
51	3/6	8/3/2016	Class of One-step majority logic decodable codes	„		
52	4/6	14/3/2016	Two-step majority logic decoding	„		
53	5/6	14/3/2016	Multiple-step majority logic decoding.	„		
54	6/6	14/3/2016	Previous Year QP Discussion	„		
55	1/7	15/3/2016	Convolution codes: Encoding of convolutional codes	„	Assignment 3	
56	2/7	15/3/2016	Encoding of convolutional codes(Contd.)	„		
57	3/7	15/3/2016	Encoding of convolutional codes(Contd.)	„		
58	4/7	21/3/2016	Structural properties	„		
59	5/7	21/3/2016	Distance properties	„		
60	6/7	21/3/2016	Viterbi decoding algorithm for decoding	„		
61	7/7	22/3/2016	Soft output Viterbi algorithm	„		
62	8/7	22/3/2016	Stack and Fano sequential decoding algorithms	„		
63	9/7	22/3/2016	Majority logic decoding. Previous Year QP Discussion.	„		
64	1/8	28/3/2016	Concatenated codes and Turbo codes: Single level concatenated codes, Multilevel concatenated codes,	„		
65	2/8	28/3/2016	Soft decision multistage decoding	„		
66	3/8	28/3/2016	Concatenated coding schemes with convolutional inner codes	„		
67	4/8	29/3/2016	Introduction to Turbo coding	„		
68	5/8	29/3/2016	Distance properties of Turbo Coding	„		
69	6/8	29/3/2016	Design of Turbo codes and Previous Year QP Discussion.	„		
70	1/9	4/4/2016	Burst - error - Correcting codes: - Burst and random error correcting codes	„	Assignment 4	

71	2/9	4/4/2016	Concept of interleaving, Cyclic codes for burst error correction – Fire codes	Board, chalk, duster		
72	3/9	4/4/2016	Convolutional codes for burst error correction	„		
73	-	5/4/2016	Revision and QP Discussion	„		
75	-	5/4/2016	Revision and QP Discussion	„		
76	-	5/4/2016	Revision and QP Discussion	„		

Signature of faculty

Signature of HOD

Signature of Principal

Department of Telecommunication

SEMESTER : Mtech 4th sem
BRANCH : TCE
SUBJECT : ACN
SUBJECT CODE :
NO OF HRS/WK : 4

NAME OF THE FACULTY : Miss Shruthi M
DATE OF COMMENCEMENT : 05.01.2016
DATE OF CLOSING : 11.04.2016
CLASS STRENGTH : 11
TOTAL HRS : 50

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	1/1	05.01.16	Unit-1- INTRODUCTION TO COMMUNICATION NETWORKS	Board, chalk, duster		
2	2/1	05.01.16	Telephone networks	„		
3	3/1	06.01.16	Computer networks	„		
4	4/1	11.01.16	Multiple access	„		
5	5/1	11.01.16	FDM, TDM, SM	„		
6	6/1	12.01.16	Networking principles	„	Assignment- I	
7	1/2	12.01.16	Unit -2 LAN ETHERNET	„		
8	2/2	18.01.16	Token ring	Board, chalk, duster		

9	3/2	18.01.16	FDDI	„		
10	4/2	19.01.16	Circuit switching	„		
11	5/2	19.01.16	Packet switching	„		
12	6/2	25.01.16	Multicasting	„	Assignm ent -II	
14	1/3	01.02.16	Unit –3 Scheduling	„		
15	2/3	01.02.16	Performance bounds			
16	3/3	02.02.16	Best effort disciplines			
17	4/3	02.02.16	Naming and addressing			
18	5/3	08.02.16	Protocol stack	„		
19	6/3	08.02.16	SDH & SONET	„	Assignm ent –III	
21	1/4	09.02.16	Unit-4 ATM NETWORKS	„		
22	2/4	09.02.16	AAL	„		
23	3/4	15.02.16	Virtual circuits			
24	4/4	15.02.16	SSCOP	Board, chalk, duster		
25	5/4	16.02.16	Internet addressing	„		
26	6/4	16.02.16	Routing, endpoint control	„	Assignm nt –IV	
27	1/5	22.02.16	Unit 5 Internet Protocol	„		
28	2/5	22.02.16	IP	„		
29	3/5	23.02.16	TCP	„		
30	4/5	23.02.16	UDP	„		
31	5/5	29.02.16	ICMP	„		
32	6/5	29.02.16	HTTP	„	Assignm ent -V	

33	1/6	01.03.16	Unit-6 TRAFFIC MANAGEMENT	Board, chalk, duster		
34	2/6	07.03.16	Models	„		
35	3/6	07.03.16	Classes	„		
36	4/6	08.03.16	Scheduling	„	Assignment 6	
40	1/7	08.03.16	Unit-7 CONTROL OF NETWORKS	„		
41	2/7	14.03.16	QoS, static dynamic routing	„		
42	3/7	14.03.16	Markov chains	„		
43	4/7	15.03.16	Queuing models	„		
44	5/7	15.03.16	Bellman ford algorithm	„		
45	6/7	21.03.16	Dijkstra's algorithm	„		
46	7/7	21.03.16	Window & rate congestion control	„		
47	8/7	22.03.16	Queue & network, control of ATM networks	„		
53		28.03.17	Revision of Unit -1	„		
54		28.03.17	Revision of Unit – 2	„		
55		29.03.16	Revision of Unit –3	„		
56		29.03.16	Revision of Unit –4	„		
57		04.04.16	Revision of Unit –5	„		
58		04.04.16	Revision of Unit –6	„		
59		05.04.16	Revision of Unit –7	„		

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