#132, AECS Layout, IT Park Road, Kundalahalli, Bangalore – 560 037

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CMR INSTITUTE

OF TECHNOLOGY

Session wise – Lesson Plan

Department of Electronics and Telecommunication

Subject Code: 14ELD41 **Subject Name: ADVANCED COMPUTER ARCHITECTURE**

SEMESTER	**: IV**	**NAME OF THE FACULTY**	**: Mrs. Shet Reshma P**
BRANCH	**: MTECH (Digital Electronics)**	**DATE OF COMMENCEMENT**	**: 11/01/2016**
SUBJECT	**: ACA**	**DATE OF CLOSING**	**:**
SUBJECT CODE	**: 14ELD41**	**CLASS STRENGTH**	**: 10**
NO OF HRS/WK	**: 5**	**TOTAL HRS**	**: 64**

Session No.	Session/ Chapter no (No of hours planned for the chapter)	Date	Topics planned for the session	Teaching Aids	Assignments/ Test planned for chapter
1	1/1	11.01.16 Monday	**UNIT1**: Prerequisite topic, Course Over view, Objectives, outcomes ,CISC/RISC processor , Basics of Computer Architecture	Board, chalk, duster	Assignment No 1
2	2/1	11.01.16 Monday	Fundamentals Of Computer Design: Classes of computers	"	
3	3/1	11.01.16 Monday	Defining a computer architecture	"	
4	4/1	12.01.16 Tuesday	Instructions set Architecture (ISA), Trends in Technology	"	
5	5/1	12.01.16	Trends in power and energy in IC's, Trends in cost	"	

		Tuesday			
6	6/1	18.01.16 Monday	Problem solving –in cost of IC's, Dependability	"	
7	7/1	18.01.16 Monday	Measuring, Reporting and Summarizing Performance	"	
8	8/1	18.01.16 Monday	Quantitative Principles of Computer Design, Fallacies and Pitfalls	"	
9	9/1	19.01.16 Tuesday	Processor Performance Equation, Amdahl's law and problems.	"	
10	1/2	19.01.16 Tuesday	**UNIT2:** Instruction Level Parallelism Concepts and Challenges	Board, chalk, duster	Assignment No 2
11	2/2	25.01.16 Monday	Various Dependences and Hazards	"	
13	3/2	25.01.16 Monday	Reducing Branch Costs with Prediction	PPT	
14	4/2	25.01.16 Monday	Dynamic Scheduling	PPT	
15	5/2	01.02.16 Monday	Dynamic Scheduling using Tomasulo's algorithm	PPT	
16	6/2	01.02.16 Monday	Exploiting ILP using Multiple Issue and Static Scheduling	PPT	
17	7/2	01.02.16 Monday	Fallacies and Pitfalls Branch Target Buffers	PPT	
18	8/2	02.02.16 Tuesday	Value Prediction, Case Study of Pentium 4,	PPT	
19	9/2	02.02.16 Tuesday	Limitations of ILP	Board, chalk, duster	
20	10/2	08.02.16 Monday	Pipelining Introduction	"	
21	11/2	08.02.16 Monday	Hazards Data Hazards, Structural Hazards, Control Hazards	"	

22	12/2	08.02.16 Monday	How is Pipelining Implemented?	“	Assignment No 3
23	13/2	09.02.16 Tuesday	What Makes Pipelining Hard to Implement,	“	
24	14/2	09.02.16 Tuesday	Crosscutting Issues	“	
25	15/2	15.02.16 Monday	Fallacies and Pitfalls with respect to Pipelining.	“	
26	1/3	15.02.16 Monday	**UNIT 3:** Memory Hierarchy Design Storage Systems. Cross Cutting issues in design of memory hierarchies	PPT	Assignment No 4
27	2/3	15.02.16 Monday	AMD Opteron Case Study	“	
28	3/3	16.02.16 Tuesday	Fallacies and Pitfalls	“	
29	4/3	16.02.16 Tuesday	Introduction to Storage System	Board, chalk, duster	
30	5/3	22.02.16 Monday	Advanced topics in disk storage	“	
31	6/3	22.02.16 Monday	Definition and examples of real faults and failures	“	
32	7/3	22.02.16 Monday	I/O performance, reliability measures and Benchmarks,	“	
33	8/3	23.02.16 Tuesday	Little Queuing Theory	“	
34	9/3	23.02.16 Tuesday	Crosscutting Issues	“	
35	10/3	29.02.16 Monday	Internet Archive Cluster	PPT	
36	11/3	29.02.16 Monday	NetApp FSA6000 Filer Case Study	PPT	
37	12/3	29.02.16 Monday	Fallacies and Pitfalls	Board, chalk, duster	
38	1/4	01.03.16 Tuesday	**UNIT 4:** Exploiting Instruction Level Parallelism statically	PPT	

39	2/4	01.03.16 Tuesday	Detecting and Enhancing Loop Level Parallelism	“	
40	3/4	08.03.16 Tuesday	Scheduling and Structuring the code for Parallelism	“	Assignment No 5
41	4/4	08.03.16 Tuesday	Hardware Support for exposing parallelism; Predicted Instructions	“	
42	5/4	21.03.16 Monday	Hardware Support for Compiler Speculation	“	
43	6/4	21.03.16 Monday	Intel IA-64 Architecture	“	
44	1/5	21.03.16 Monday	**UNIT 5:** Introduction, InterProcessor Communication	PPT	
45	2/5	22.03.16 Tuesday	Characteristics of Scientific Applications	“	
46	3/5	22.03.16 Tuesday	Performance of Scientific Applications on Shared Memory Multiprocessor	“	Assignment No 6
47	4/5	28.03.16 Monday	Performance measurement of Parallel processors with Scientific applications	“	
48	5/5	28.03.16 Monday	Implementing Cache Coherence	“	
49	6/5	28.03.16 Monday	The Custom Cluster Approach	“	
50	1/6	29.03.16 Tuesday	**UNIT 6:**Computer Arithmetic Introduction	Board, chalk, duster & PPT	
51	2/6	29.03.16 Tuesday	Basic Techniques of Integer Arithmetic	“	Assignment No 7
52	3/6	04.04.16 Monday	Floating point, Floating Point Multiplication	“	
53	4/6	04.04.16 Monday	Floating point Addition, Division	“	
54	5/6	04.04.16 Monday	Speeding up Integer Addition	“	
55	6/6	05.04.16 Tuesday	Speeding up Integer Multiplication	“	
56	7/6	05.04.16	Division	“	

		Tuesday			
57	8/6	11.04.16 Monday	Fallacies and Pitfalls	“	
58	9/6	11.04.16 Monday	Hardware Speculation	Board, chalk, duster	
59	10/6	11.04.16 Monday	Itanium processor	“	
60	11/6	12.04.16 Tuesday	Revision of Module 1	“	
61	12/6	12.04.16 Tuesday	Problem Solving	“	
62	13/6	18.04.16 Monday	Discussing topics from Question Paper	“	
63	14/6	18.04.16 Monday	Revision of Module 2,3	“	
64	15/6	18.04.16 Monday	Revision of Module 4,5	“	

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication

SEMESTER : IV (MTECH)
SECTIONS :
SUBJECT : Advances in VLSI design
SUBJECT CODE : 14EVE421
NO OF HRS/WK : 5

NAME OF THE FACULTY : Mr. MAHESH S GOUR
DATE OF COMMENCEMENT : 18.01.2016
DATE OF CLOSING : 11.04.2016
CLASS STRENGTH : 17
TOTAL HRS : 54

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	18/01	Fundamentals of CMOS, Digital Design	Board, chalk, duster		
2	**2/1**	18/01	Super buffers, Bi-CMOS and Steering logic: Introduction, RC delay lines	,,		
3	**3/1**	19/01	Super buffers-An NMOS super buffer	,,		
4	**4/1**	19/01	CMOS super buffers	,,		
5	**5/1**	19/01	Tri state super buffer and pad drivers	,,		
6	**6/1**	25/01	Dynamic ratio less inverters	,,		
7	**7/1**	25/01	Large capacitive loads	,,		
8	**8/1**	25/02	Pass logic, Designing of transistor logic	Board, chalk, duster		
9	**9/1**	01/02	General functional blocks – NMOS and CMOS func blocks	,,		
10	**1/2**	01/02	Special circuit layouts and technology mapping:	,,		

			Introduction			
11	**2/2**	02/02	Tally circuits	,,		
12	**3/2**	02/02	NAND-NAND			
13	**4/2**	02/02	NOR-NOR & AOI logic	,,		
14	**5/2**	08/02	NMOS,CMOS multiplexers	,,		
15	**6/2**	08/02	Barrel shifter, Wire routing & module layout	,,		
16	**1/3**	09/02	MESFETS: MESFET & MODFET operations			
17	**2/3**	09/02	MESFETS: MESFET & MODFET operations(cntd.)		Assignment 1	
18	**3/3**	09/02	Quantitative description of MESFETS			
19	**4/3**	15/02	Quantitative description of MESFETS(cntd)	,,		
20	**5/3**	15/02	Problems	,,		
21	**1/4**	16/02	Review of MOS circuit: MOS& CMOS static plots	,,		
22	**2/4**	16/02	MOS& CMOS static plots (cntd.)	,,	Assignment 2	
23	**3/4**	16/02	Switches	,,		
24	**4/4**	22/02	Comparison b/w CMOS & BI CMOS			
25	**5/4**	22/02	Fabrication process			
26	**1/5**	23/02	MIS Structures and MOSFETS:MIS system in equilibrium	Board, chalk, duster		
27	**2/5**	23/02	MIS Structures and MOSFETS:MIS system in equilibrium(contd..)	,,		
28	**3/5**	23/02	MIS system under bias	,,		
29	**4/5**	29/02	MIS system under bias (contd..)	,,	Assignment 3	
30	**5/5**	29/02	Basic Theory of MOSFET operation	,,		

31	**6/5**	01/03	Basic Theory of MOSFET operation (contd..)	,,		
32	**7/5**	01/03	Small Signal operation of MESFETS & MOSFETS	,,		
33	**8/5**	01/03	Small Signal operation of MESFETS & MOSFETS (contd..)	,,		
34	**1/6**	08/03	Short channel effect and challenges to CMOS: Short channel effects	,,	Assignment 4	
35	**2/6**	08/03	Short channel effects(cntd)	Board, chalk, duster		
36	**3/6**	14/03	Scaling Theory	,,		
37	**4/6**	14/03	Scaling Theory (contd..)	,,		
38	**5/6**	14/03	Processing challenges to further CMOS miniaturization	,,		
39	**1/7**	15/03	Beyond CMOS: Evolutionary advances beyond CMOS	,,		
40	**2/7**	15/03	Carbon Nanotubes	,,		
41	**3/7**	21/03	Carbon Nanotubes (contd..)	,,		
42	**4/7**	21/03	Conventional vs tactile computing	,,	Assignment 5	
43	**5/7**	21/03	Computing molecular and biological computing mole electronics			
44	**6/7**	22/03	Molecular diode and diode – diode logic	,,		
45	**7/7**	22/03	Molecular diode and diode – diode logic (contd..)	,,		
46	**8/7**	28/03	Defect tolerant computing	,,	Assignment 6	
47	**1/8**	28/03	System design: CMOS design methods ,Structured design methods	,,		
48	**2/8**	28/03	Strategies encompassing hierarchy, Regularity, Modularity & locality	,,		
49	**3/8**	29/03	CMOS chip design options	,,		

50	**4/8**	29/03	Programmable logic, Programmable Interconnect	,,		
51	**5/8**	04/04	Programmable Structure	,,	Assignment 7	
52	**6/8**	04/04	Gate arrays standard cell approach			
53	**7/8**	04/04	Gate arrays standard cell approach (contd..)	Board, chalk, duster		
54	**8/8**	05/04	Full custom approach	,,		

Signature of faculty Signature of HOD Signature of Principal