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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication

SEMESTER	2nd sem	Name of Faculty	CHETAN H
SECTIONS	VLSI	Date of Commencement	1/2/2016
Subject	AMVLSI	Date of Closing	10/05/2016
Subject Code	14EVE21	Class Strength	23
No of Hrs/Week	5	Total Hours	53

Session No	Chapter no (No of hrs planed for the chapter)	**Class #**	**Topic**	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	First two classes	Basics of MOSFET	White Board, duster		
2	**1/1**			,,		
3	**2/2**	1-2	General considerations, MOS I/V Characteristics	,,		
4	**2/2**	3-4	Second order effects, MOS device models.	,,		
5	**3/2**	5-6	CS stage with resistance load, divide connected load	,,		
6	**3/2**	7-11	current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models.	,,		
7	**3/1**	12-13	source follower, Common gate stage	,,		
8	**4/1**	14-16	Cascade stage and Difference pair	White Board, duster		

9	**4/2**	17-18	Noise in CS stage, C- G stage	,,		
10	**4/1**	19	source follower, cascade stage	,,		
11	**4/1**	20	differential pair.	,,		
12	**4/1**	16-17	Basic difference pair, common mode response			
13	**4/1**	18-19	Differential pair with MOS loads, Gilbert cell	,,		
14	**4/1**	20-22	Basic current mirrors, Cascade mirrors, active current mirrors	,,		
15	**5/1**	20	One Stage OP-Amp,	,,		
16	**5/2**	21-22	Two Stage OP-Amp, Gain boosting,			
17	**5/1**	23-24	Common Mode Feedback, Slew rate		Assignment 1	
18	**5/1**	25-27	Power Supply Rejection, Noise in Op Amps.			
19	**5/2**	28-29	Ring Oscillators, LC Oscillators	,,		
20	**6/1**	29-30	VCO, Mathematical Model of VCO	,,		
21	**6/2**	31-32	Simple PLL, Charge pump PLL,	,,		
22	**6/1**	32-35	Non-ideal effects in PLL, Delay locked loops and applications.	,,	Assignment 2	
23	**6/2**	36-37	General Considerations, Supply Independent biasing	,,		
24	**6/1**	38-40	PTAT Current Generation, Constant Gm Biasing			
25	**7/3**	41-43	Sampling Switches, Switched Capacitor Amplifiers.			
26	**7/1**	44-46	DAC & ADC Specifications, Resistor String DAC	White Board, duster		
27	**7/2**	47-48	R-2R Ladder Network, Current Steering DAC	,,		
28	**8/2**	49	Charge Scaling DAC, Cyclic DAC	,,		

29	**8/4**	50-53	Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.	,,	Assignment 3	

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication

SEMESTER	2nd sem	Name of Faculty	CHETAN H
SECTIONS	VLSI	Date of Commencement	1/2/2016
Subject	LOW Power	Date of Closing	10/05/2016
Subject Code	14EVE22	Class Strength	23
No of Hrs/Week	5	Total Hours	65

Session No	Chapter no (No of hrs planed for the chapter)	**Class #**	**Topic**	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	First two classes -Pre requisites	Fundamentals of CMOS, Digital design	White Board, duster		
2	**1/1**			,,		
3	**1/2**	1-2	Introduction: Need for low power VLSI chips.	,,		
4	**1/2**	3-4	Source of power dissipation on Digital integrated circuit.	,,		
5	**1/2**	5-6	Emerging low power approaches	,,		
6	**1/4**	7-11	Physics of power dissipation in cmos devices. Device technology impact on low power	,,		
7	**2/1**	12-13	Dynamic power dissipation in CMOS	,,		
8	**2/1**	14-16	Transistor sizing & gate oxide thickness,	White Board, duster		
9	**2/2**	17-18	Impact of technology Scaling,	,,		

10	**2/1**	19	Technology & Device innovation	,,		
11	**3/1**	20	**Power estimation, Simulation Power analysis**: SPICE circuit simulators,	,,		
12	**3/1**	16-17	Gate level logic simulation, capacitive power estimation,			
13	**3/1**	18-19	Static state power, gate level capacitance estimation,	,,		
14	**3/1**	20-22	Architecture level analysis. Data correlation analysis in DSP systems	,,		
15	**3/1**	20	Monte Carlo simulation	,,		
16	**4/2**	21-22	**Probabilistic power analysis**: Random logic signals			
17	**4/1**	23-24	Probability & frequency		Assignment 1	
18	**4/1**	25-27	Probabilistic power analysis techniques,			
19	**4/2**	28-29	Signal entropy	,,		
20	**5/1**	29-30	**Low Power Design Circuit level**: Power consumption in circuits.	,,		
21	**5/2**	31-32	Flip Flops & Latches design	,,		
22	**5/1**	32-35	High capacitance nodes, Low power digital cells library	,,	Assignment 2	
23	**5/2**	36-37	**Logic level:** Gate reorganization	,,		
24	**5/1**	38-40	Signal gating, logic encoding			
25	**5/3**	41-43	State machine encoding			
26	**5/1**	44-46	Pre-computation logic	White Board, duster		
27	**6/1**	47	**Low power Architecture & Systems:** Power & performance management,	,,		
28	**6/1**	48	Switching activity reduction	,,		
29	**6/1**	49	Parallel architecture with voltage reduction	,,	Assignment 3	
30	**6/1**	50	Flow graph transformation, 43 Low power arithmetic components			
31	**6/2**	51-52	Low power memory design.	White Board, duster		

32	**7/2**	52-53	**Low power Clock Distribution:** Power dissipation in clock distribution	,,		
33	**7/2**	53-54	Single driver Vs distributed buffers Zero skew Vs tolerable skew,	,,		
34	**7/2**	55-56	Chip and package co design of clock network	,,		
35	**8/2**	57-58	**Algorithm & Architectural Level Methodologies:** Introduction	White Board, duster		
36	**8/2**	59-60	Design flow	,,		
37	**8/3**	61-63	Algorithmic level analysis & optimization,	,,		
38	**8/2**	64-65	Architectural level estimation & synthesis	,,		
39	**-/-**	66-69	Revision	--	-	-

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication

SEMESTER : II (MTECH)
SECTIONS :
SUBJECT : Real Time Operating Systems
SUBJECT CODE : 14ELD24
NO OF HRS/WK : 5

NAME OF THE FACULTY : Sudatta Mohanty
DATE OF COMMENCEMENT : 01.02.2016
DATE OF CLOSING : 15.05.2016
CLASS STRENGTH : 36
TOTAL HRS : 45

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	01/02	Brief history of Real Time Systems,	Board, chalk, duster		
2	**2/1**	03/02	A brief history of Embedded Systems, Resource Analysis	,,		
3	**3/1**	04/02	Real-Time Service Utility, Scheduling Classes	,,		
4	**4/1**	05/02	The Cyclic Executive	,,		
5	**5/1**	09/02	Scheduler Concepts,	,,		
6	**6/1**	10/02	Preemptive Fixed Priority	,,		
7	**7/1**	12/02	Scheduling Policies, Real-Time OS	,,		
8	**8/1**	13/02	Thread Safe Reentrant Functions.	Board, chalk, duster		
9	**9/1**	16/02	Fixed-Priority Policy,	,,		
10	**1/2**	17/02	Rate Monotonic least upper bound	,,		

11	**2/2**	22/02	Feasibility, Necessary and Sufficient feasibility	,,		
12	**3/2**	23/02	Deadline – Monotonic Policy, Dynamic priority policies.			
13	**4/2**	25/02	Intermediate I/O, , I/O Architecture	,,		
14	**5/2**	26/02	Execution efficiency, Worst-case Execution time,	,,		
15	**6/2**	01/03	Physical hierarchy	,,		
16	**1/3**	02/03	Capacity and allocation, Shared Memory			
17	**2/3**	04/03	ECC Memory, Flash file systems.		Assignment 1	
18	**3/3**	05/03	Blocking, Deadlock and livestock			
19	**4/3**	09/03	Critical sections to protect shared resources,	,,		
20	**5/3**	10/03	priority inversion, Problems,	,,		
21	**1/4**	17/03	Missed Deadlines, QoS	,,		
22	**2/4**	18/03	Alternatives to rate monotonic policy	,,	Assignment 2	
23	**3/4**	21/03	Mixed hard and soft real-time services.	,,		
24	**4/4**	22/03	Firmware components			
25	**5/4**	24/03	RTOS system software mechanisms			
26	**1/5**	28/03	Software application components.	Board, chalk, duster		
27	**2/5**	30/03	Execptions assert, Checking return codes	,,		
28	**3/5**	31/03	Single-step debugging, kernel scheduler traces	,,		
29	**4/5**	04/04	Test access ports, Trace ports	,,	Assignment 3	
30	**5/5**	06/04	Power-On self test and diagnostics	,,		
31	**6/5**	07/04	External test equipment, Application-level debugging	,,		

32	**7/5**	12/04	Basic concepts of drill-down tuning,	,,		
33	**8/5**	13/04	hardware – supported profiling and tracing	,,		
34	**1/6**	16/04	Building performance monitoring into software,	,,	Assignment 4	
35	**2/6**	18/04	Path length,	Board, chalk, duster		
36	**3/6**	21/04	Path length, (contd)	,,		
37	**4/6**	22/04	Efficiency, and Call frequency	,,		
38	**5/6**	28/04	Call frequency(contd)	,,		
39	**1/7**	29/04	Fundamental optimizations,	,,		
40	**2/7**	02/05	Reliability and Availability, Similarities and differences	,,		
41	**3/7**	03/05	Reliability, Reliable software, Available software,	,,		
42	**4/7**	05/05	PIC microcontroller	,,	Assignment 5	
43		07/05	Revision of unit1-4			
44		10/05	Revision of unit4-8			
45		11/05	Revision of unit8-12			

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Telecommunication

SEMESTER : II
BRANCH : TCE
SUBJECT : SOC Design
SUBJECT CODE : 14EVE255
NO OF HRS/WK : 5

NAME OF THE FACULTY : Bhumika Narang
DATE OF COMMENCEMENT : 01.02.2016
DATE OF CLOSING : 11.5.2016
CLASS STRENGTH : 21
TOTAL HRS : 56

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	01-02-2016	Introduction of System on Chip Design and course outline	Board, chalk, duster		
2	**2/1**	02-02-2016	Moore's Law and CMOS scaling	,,		
3	**3/1**	04-02-2016	Benefits of system on chip Integration in terms of Cost, Power and Performance	,,		
4	**4/1**	05-02-2016	Comparison on SOB, SOC, SIP	,,		
5	**5/1**	08-02-2016	Goals of SOC Design	,,		
6	**6/1**	09-02-2016	IP based Design and Design Reuse	,,		
7	**7/1**	10-02-2016	Revision of Unit-1	,,	Assignment- I	
8	**1/2**	12-02-2016	Canonical SOC Design	Board, chalk, duster		
9	**2/2**	15-02-2016	Water fall SOC Design flow	,,		
10	**3/2**	16-02-2016	Spiral SOC Design flow	,,		

11	**4/2**	17-02-2016	Top-down Vs Bottom-up approaches and Specification requirement	,,		
12	**5/2**	22-02-2016	Types of Specification	,,		
13	**6/2**	23-02-2016	System Design Process	,,		
14	**7/2**	24-02-2016	System Level Design Issues: Standard Model	,,		
15	**8/2**	25-02-2016	Soft IP Vs. Hard IP			
16	**9/2**	26-02-2016	The role of full custom design in reuse			
17	**10/2**	01-03-2016	Verification of SOCs			
18	**11/2**	02-03-2016	Integration with SOCs	,,	Assignment -II	
19	**12/2**	03-03-2016	Hardware and - software co design	,,		
20	**13/2**	04-03-2016	Design for Timing Closure	,,		
21	**14/2**	05-03-2016	Interface and Timing Closure	,,		
22	**15/2**	09-03-2016	Macro Interfaces	,,		
23	**16/2**	10-03-2016	Sub block Interfaces			
24	**17/2**	11-03-2016	Design for Timing Closure	Board, chalk, duster		
25	**18/2**	17-03-2016	Logic Design Issues	,,		
26	**19/2**	18-03-2016	Floor planning	,,	Assignment –III	
27	**20/2**	21-03-2016	Logic Design Issues	,,		
28	**21/2**	22-03-2016	Synthesis strategy	,,		
29	**22/2**	23-03-2016	Timing budgets	,,		
30	**23/2**	24-03-2016	Hard Macros and Clock Distribution and Verification Strategy	,,		
31	**24/2**	28-03-2016	On Chip Buses	,,		

32	**25/2**	30-03-2016	System Interconnect and On Chip Buses	,,		
33	**26/2**	31-03-2016	Basic Interface Issues, IP to Ip interfaces	Board, chalk, duster	Assignment -IV	
34	**27/2**	01-04-2016	On Chip Debug Structures	,,		
35	**28/2**	02-04-2016	Designing for Low Power Circuits, Lowering the supply voltage	,,		
36	**29/2**	04-04-2016	Reduction of capacitance and switching activity	,,		
37	**30/2**	06-04-2016	Memory Architecture and clock distribution	,,		
38	**31/2**	07-04-2016	Hardware Accelerators in SOC	,,		
39	**32/2**	11-04-2016	Revision of Unit -2	,,		
40	**33/2**	12-04-2016	Introduction of MPSOCs, What, Why and How of MPSOCs	,,		
41	**34/2**	13-04-2016	Design Methodologies of MPSOCs	,,		
42	**35/2**	16-02-2016	Performance, Flexibility and Optimization Viewpoint of MPSOCs	,,	Assignmnt –V	
43	**1/5**	18-04-2016	Revision of Unit - 5	,,		
44	**2/5**	20-04-2016	Embedded Memories - Cache Memories	,,		
45	**3/5**	21-04-2016	Flash Memories, Embedded DRAM	,,		
46	**4/5**	22-04-2016	Cache Coherence	,,		
47	**1/3**	28-04-2016	MESI Protocol and Directory based Coherence	,,		
48	**2/3**	29-04-2016	Revision of Unit - 3	,,		
49	**3/3**	30-04-2016	Interconnect Architecture of SOC: Bus Architecture and its limitations	Board, chalk, duster		
50	**4/3**	02-04-2016	Network on chip topologies	,,	Assignmnt –VI	
51	**5/3**	03-04-2016	Mesh based NOC and Routing of NOC	,,		

52	**6/3**	05-04-2016	Packet Switching	,,		
53	**1/4**	06-04-2016	Wormhole Routing	,,		
54	**2/4**	07-04-2016	Revision of Unit- 4	,,	Assignmnt –VII	
55	**3/4**	10-04-2016	Case Study : A low power open multimedia application platform for 3G wireless networks : Platform Core Architecture	IEEE Paper		
56	**4/4**	11-04-2016	Case Study : A low power open multimedia application platform for 3G wireless networks : Platform Software Architecture	IEEE Paper		

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Telecommunication

SEMESTER : II
BRANCH : TCE
SUBJECT : VLSI Testing and Verification
SUBJECT CODE : 14EVE255
NO OF HRS/WK : 5

NAME OF THE FACULTY : Bhumika Narang
DATE OF COMMENCEMENT : 01.02.2016
DATE OF CLOSING : 11.5.2016
CLASS STRENGTH : 21
TOTAL HRS : 56

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	01-02-2016	Introduction to VLSI Testing and Verification & Testing Philosophy	Board, chalk, duster		
2	**2/1**	03-02-2016	Role of Testing & Digital and Analog VLSI Testing	,,		
3	**3/1**	03-02-2016	VLSI technology trends affecting testing and Faults in Digital Circuits	,,		
4	**4/1**	05-02-2016	Failures and Faults & Modeling of Faults	,,		
5	**5/1**	08-02-2016	Delay Faults and Temporary Faults	,,		
6	**6/1**	09-02-2016	Revision of Unit – 1	,,		
7	**1/2**	11-02-2016	Fault Diagnosis of Digital circuits and Test generation techniques for combinational circuits and One Dimensional Path Sensitization	,,	Assignment- I	
8	**2/2**	11-02-2016	Boolean Difference	Board, chalk, duster		

9	**3/2**	13-02-2016	D – Algorithm	,,		
10	**4/2**	15-02-2016	Path Oriented Decision Making (PODEM), FAN & Delay fault detection	,,		
11	**5/2**	16-02-2016	Detection of multiple faults in combinational logic circuits & Revision of Unit 2	,,		
12	**6/2**	18-02-2016	Controllability and Observability & Ad Hoc Design rules for improving Testability	,,		
13	**7/2**	18-02-2016	Design of Diagnosable Sequential circuits	,,		
14	**1/3**	23-02-2016	Scan Path Technique for testable sequential circuit design	,,		
15	**2/3**	24-02-2016	Level- Sensitive Scan Design and Random Access Scan Technique			
16	**3/3**	25-02-2016	Partial Scan and Testable Sequential circuits design using non scan techniques			
17	**4/3**	29-02-2016	Cross Check & Boundary Scan			
18	**5/3**	29-02-2016	BIST : Test pattern generation for BIST : Exhaustive Testing	,,	Assignment -II	
19	**6/3**	02-03-2016	Pseudo Exhaustive Pattern Generation	,,		
20	**7/3**	03-03-2016	Pseudo Random Pattern Generator and Deterministic Testing	,,		
21	**8/3**	04-03-2016	Output Response Analysis : Transition Count & Syndrome Checking	,,		
22	**9/3**	08-03-2016	Output Response Analysis : Signature Analysis, Circular BIST	,,		
23	**10/3**	08-03-2016	BIST Architecture : BILBO & STUMPS			
24	**11/3**	10-03-2016	BIST Architecture : LOCST			
25	**12/3**	11-03-2016	Revision of Unit 3			
26	**13/3**	17-03-2016	What is Verification, What is a Test Bench and the importance of verification			

27	**14/3**	19-03-2016	Reconvergence Model & Formal Verification			
28	**15/3**	19-03-2016	Equivalence Checking, Model Checking and Functional Verification			
29	**16/3**	22-03-2016	Revision of Unit – 5			
30	**17/3**	23-03-2016	Verification Tools: Linting Tools and its limitations		Assignment –III	
31	**1/5**	24-03-2016	Linting Verilog source code and Linting VHDL source code			
32	**2/5**	29-03-2016	Linting open vera and e-source code	Board, chalk, duster		
33	**3/5**	29-03-2016	Code Reviews and Simulators : Stimulus and Response, Event based and Cycle based simulations	,,		
34	**4/5**	31-03-2016	Co- Simulators and Verification Intellectual Property : Hardware Modelers	,,		
35	**5/5**	01-04-2016	Waveform Viewers and Code Coverage	,,		
36	**1/6**	02-04-2016	Revision of Unit – 6	,,	Assignment -IV	
37	**2/6**	05-04-2016	The Role of the Verification Plan and Defining First Time Success	,,		
38	**3/6**	05-04-2016	Levels of Verification : Unit Level Verification & Reusable Components Verification	,,		
39	**4/6**	07-04-2016	ASIC and FPGA verification	,,		
40	**5/6**	11-04-2016	System Level and Board Level Verification, Verification Strategies and Verifying the response	,,		
41	**6/6**	12-04-2016	Revision of Unit - 7	Board, chalk, duster		
42	**7/6**	15-04-2016	Concept of Static Timing Analysis, Cross talk and Noise & Limitation of STA	,,		
43	**8/6**	15-04-2016	Slew of a wave form and Skew between the signals, Min and Max timing paths	,,		

44	**1/7**	18-04-2016	Clock domains and Operating conditions	,,		
45	**2/7**	20-04-2016	Critical path analysis and Falsepaths, Timing Models	,,		
46	**3/7**	21-04-2016	BIST Techniques for RAM Chips	,,		
47	**4/7**	23-04-2016	Revision of Unit -8	,,		
48	**5/7**	23-04-2016	Physical Design Verification : Layout rule checks and Electrical rule checks	,,	Assignmnt –V	
49	**6/7**	29-04-2016	Parasitic Extraction and Antenna	,,		
50	**1/8**	30-04-2016	Crosstalk and Noise : Crosstalk glitch analysis	,,		
51	**2/8**	02-04-2016	Crosstalk Delay analysis and Timing Verification	,,		
52	**3/8**	04-04-2016	Revision of Unit - 9	,,		
53	**4/8**	04-04-2016	Testable Memory Design : RAM Fault Models	,,		
54	**5/8**	06-04-2016	Test Algorithms for RAMs : GALPAT, Walking 0s and 1s, March Test, Checkerboard Test	,,	Assignmnt –VI	
55	**6/8**	07-04-2016	Detection of Pattern Sensitive Faults and BIST Techniques for RAM Chips	,,		
56	**7/8**	10-04-2016	Test Generation and BIST for Embedded RAMs Revision of Unit - 4	,,		

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