#132, AECS Layout, IT Park Road, Kundalahalli, Bangalore – 560 037
T:+9180 28524466 / 77

CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication

SEMESTER : IV (MTECH)
SECTIONS :
SUBJECT : Advances in VLSI design
SUBJECT CODE : 14EVE421
NO OF HRS/WK : 5

NAME OF THE FACULTY : Mr. MAHESH S GOUR
DATE OF COMMENCEMENT : 18.01.2016
DATE OF CLOSING : 11.04.2016
CLASS STRENGTH : 17
TOTAL HRS : 54

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	18/01	Fundamentals of CMOS, Digital Design	Board, chalk, duster		
2	**2/1**	18/01	Super buffers, Bi-CMOS and Steering logic: Introduction, RC delay lines	,,		
3	**3/1**	19/01	Super buffers-An NMOS super buffer	,,		
4	**4/1**	19/01	CMOS super buffers	,,		
5	**5/1**	19/01	Tri state super buffer and pad drivers	,,		
6	**6/1**	25/01	Dynamic ratio less inverters	,,		
7	**7/1**	25/01	Large capacitive loads	,,		
8	**8/1**	25/02	Pass logic, Designing of transistor logic	Board, chalk, duster		
9	**9/1**	01/02	General functional blocks – NMOS and CMOS func blocks	,,		
10	**1/2**	01/02	Special circuit layouts and technology mapping:	,,		

			Introduction			
11	**2/2**	02/02	Tally circuits	,,		
12	**3/2**	02/02	NAND-NAND			
13	**4/2**	02/02	NOR-NOR & AOI logic	,,		
14	**5/2**	08/02	NMOS,CMOS multiplexers	,,		
15	**6/2**	08/02	Barrel shifter, Wire routing & module layout	,,		
16	**1/3**	09/02	MESFETS: MESFET & MODFET operations			
17	**2/3**	09/02	MESFETS: MESFET & MODFET operations(cntd.)		Assignment 1	
18	**3/3**	09/02	Quantitative description of MESFETS			
19	**4/3**	15/02	Quantitative description of MESFETS(cntd)	,,		
20	**5/3**	15/02	Problems	,,		
21	**1/4**	16/02	Review of MOS circuit: MOS& CMOS static plots	,,		
22	**2/4**	16/02	MOS& CMOS static plots (cntd.)	,,	Assignment 2	
23	**3/4**	16/02	Switches	,,		
24	**4/4**	22/02	Comparison b/w CMOS & BI CMOS			
25	**5/4**	22/02	Fabrication process			
26	**1/5**	23/02	MIS Structures and MOSFETS:MIS system in equilibrium	Board, chalk, duster		
27	**2/5**	23/02	MIS Structures and MOSFETS:MIS system in equilibrium(contd..)	,,		
28	**3/5**	23/02	MIS system under bias	,,		
29	**4/5**	29/02	MIS system under bias (contd..)	,,	Assignment 3	
30	**5/5**	29/02	Basic Theory of MOSFET operation	,,		

31	**6/5**	01/03	Basic Theory of MOSFET operation (contd..)	,,		
32	**7/5**	01/03	Small Signal operation of MESFETS & MOSFETS	,,		
33	**8/5**	01/03	Small Signal operation of MESFETS & MOSFETS (contd..)	,,		
34	**1/6**	08/03	Short channel effect and challenges to CMOS: Short channel effects	,,	Assignment 4	
35	**2/6**	08/03	Short channel effects(cntd)	Board, chalk, duster		
36	**3/6**	14/03	Scaling Theory	,,		
37	**4/6**	14/03	Scaling Theory (contd..)	,,		
38	**5/6**	14/03	Processing challenges to further CMOS miniaturization	,,		
39	**1/7**	15/03	Beyond CMOS: Evolutionary advances beyond CMOS	,,		
40	**2/7**	15/03	Carbon Nanotubes	,,		
41	**3/7**	21/03	Carbon Nanotubes (contd..)	,,		
42	**4/7**	21/03	Conventional vs tactile computing	,,	Assignment 5	
43	**5/7**	21/03	Computing molecular and biological computing mole electronics			
44	**6/7**	22/03	Molecular diode and diode – diode logic	,,		
45	**7/7**	22/03	Molecular diode and diode – diode logic (contd..)	,,		
46	**8/7**	28/03	Defect tolerant computing	,,	Assignment 6	
47	**1/8**	28/03	System design: CMOS design methods ,Structured design methods	,,		
48	**2/8**	28/03	Strategies encompassing hierarchy, Regularity, Modularity & locality	,,		
49	**3/8**	29/03	CMOS chip design options	,,		

50	**4/8**	29/03	Programmable logic, Programmable Interconnect	,,		
51	**5/8**	04/04	Programmable Structure	,,	Assignment 7	
52	**6/8**	04/04	Gate arrays standard cell approach			
53	**7/8**	04/04	Gate arrays standard cell approach (contd..)	Board, chalk, duster		
54	**8/8**	05/04	Full custom approach	,,		

Signature of faculty Signature of HOD Signature of Principal

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SUBJECT CODE : 14EVE41
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NAME OF THE FACULTY : Mr. MAHESH S GOUR
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Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	18/01	Introduction to the subject and syllabus discussion	Board, chalk, duster		
2	**2/1**	18/01	Microelectronics intro	,,		
3	**3/1**	18/01	Semiconductor technologies & circuit taxonomy	,,		
4	**4/1**	19/01	Microelectronic design styles	,,		
5	**5/1**	19/01	Intro to synthesis	,,		
6	**6/1**	25/01	Intro to optimization	,,		
7	**1/2**	25/01	Graphs: notation, undirected graphs	,,		
8	**2/2**	25/01	Directed graphs	Board, chalk, duster		
9	**3/2**	01/02	Combinatorial optimization	,,		
10	**4/2**	01/02	Combinatorial optimization (contd..)	,,		

11	**5/2**	01/02	Combinatorial optimization (contd..)	,,		
12	**6/2**	02/02	algorithms			
13	**7/2**	02/02	Tractable & intractable problems	,,		
14	**8/2**	08/02	Algorithms for linear & integer programs	,,		
15	**9/2**	08/02	Algorithms for linear & integer programs (contd..)	,,		
16	**10/2**	08/02	Graph optimization problems & algorithms			
17	**11/2**	09/02	Graph optimization problems & algorithms (contd..)		Assignment 1	
18	**1/3**	09/02	Hardware modeling languages: features			
19	**2/3**	15/02	Structural h/w languages	,,		
20	**3/3**	15/02	Behavioral h/w languages	,,		
21	**4/3**	15/02	Hdl's used in synthesis	,,		
22	**5/3**	16/02	Logic networks, state diagrams	,,	Assignment 2	
23	**6/3**	16/02	Data flow & sequencing graphs	,,		
24	**7/3**	22/02	Compilation & optimization techniques			
25	**1/4**	22/02	Logic optimization:principles			
26	**2/4**	22/02	Operation on 2 level logic	Board, chalk, duster		
27	**3/4**	23/02	Algorithms for logic minimization	,,		
28	**4/4**	23/02	Symbolic minimization	,,		
29	**5/4**	29/02	Minimization of Boolean relations	,,	Assignment 3	
30	**6/4**	29/02	Minimization of Boolean relations (contd..)	,,		
31	**1/5**	29/02	Models & transformation of comb networks	,,		

32	**2/5**	01/03	Algebraic model	,,		
33	**3/5**	01/03	Synthesis of testable network	,,		
34	**4/5**	08/03	Algorithm for delay evaluation	,,	Assignment 4	
35	**5/5**	08/03	rule based logic optimization	Board, chalk, duster		
36	**1/6**	14/03	Seq circuit optimization using state based models	,,		
37	**2/6**	14/03	Seq circuit optimization using state based models (contd..)	,,		
38	**3/6**	14/03	Seq circuit optimization using state based models (contd..)	,,		
39	**4/6**	15/03	Seq circuit optimization using state based models (contd..)	,,		
40	**1/7**	15/03	Model for scheduling problems	,,		
41	**2/7**	21/03	Scheduling with resource constraint	,,		
42	**3/7**	21/03	Scheduling without resource constraint	,,	Assignment 5	
43	**4/7**	21/03	Algorithms for extended sequencing models			
44	**5/7**	22/03	Algorithms for extended sequencing models-problems	,,		
45	**6/7**	22/03	Scheduling pipelined circuits	,,		
46	**1/8**	28/03	Problem formulation & analysis	,,	Assignment 6	
47	**2/8**	28/03	Algorithms for library binding	,,		
48	**3/8**	28/03	Rule based library binding	,,		
49	**4/8**	29/03	Problems for library binding	,,		
50	**1/9**	29/03	Simulation, Types of simulators	,,		
51	**2/9**	04/04	Components of simulator	,,	Assignment 7	
52	**3/9**	04/04	Fault simulation techniques			

53	**4/9**	04/04	ATPG	Board, chalk, duster		
54	**5/9**	05/04	DFT techniques	,,		

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