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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication Engineering

SEMESTER :I
BRANCH : ECE
SUBJECT : AESD
SUBJECT CODE : 16EVE13
NO OF HRS/WK : 4

NAME OF THE FACULTY : Mr. Mahesh S Gour
DATE OF COMMENCEMENT : 26.09.2016
DATE OF CLOSING : 20.12.2016
CLASS STRENGTH : 7
TOTAL HRS : 50

S.No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	26/9/16	**module –1** **Embedded System**: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors	Board, chalk, Duster	Prerequisite	
2	**2/1**	26/9/16	Actuators, LED, Opto coupler, Communication Interface	,,		
3	**3/1**	27/9/16	Reset circuits, RTC, WDT,	,,		
4	**4/1**	28/9/16	Characteristics and Quality Attributes of	,,	Assignment - I	

			Embedded Systems Approaches			
5	**5/1**	29/9/16	Characteristics and Quality Attributes of Embedded Systems (contd..)	,,		
6	**6/1**	30/9/16	- Characteristics and Quality Attributes of Embedded Systems(contd..)	,,		
7	**½**	1/10/16	**module –2** Hardware Software Co-Design, embedded firmware design approaches, computational models			
8	**2/2**	3/10/16	embedded firmware development languages,	,,		
9	**3/2**	4/10/16	Integration and testing of Embedded Hardware and firmware	Board, chalk, Duster		
10	**4/2**	5/10/16	Components in embedded system development environment (IDE),	,,	Assignment -II	
11	**5/2**	6/10/16	files generated during compilation	,,		
12	**6/2**	11/10/16	simulators, emulators and debugging	,,		
13	**1/3**	12/10/16	**Module –3** **ARM-32 bit Microcontroller**: Thumb-2 technology	,,		
15	**2/3**	15/10/16	applications of ARM, Architecture of ARM Cortex M3			
16	**3/3**	15/10/16	Various Units in the architecture,	,,		

17	**4/3**	19/10/16	Various Units in the architecture(contd..)	Board, chalk, Duster		
18	**5/3**	20/10/16	General Purpose Registers, Special Registers	,,	Assignment –III	
19	**6/3**	2/11/16	General Purpose Registers, Special Registers(cond..)	,,		
20	**7/3**	3/11/16	exceptions, interrupts, stack operation, reset sequence	,,		
21	¼	5/11/16	**MODULE –4** **Instruction Sets**: Assembly basics, Instruction list	,,		
22	**2/4**	6/11/16	Assembly basics, Instruction list(contd..)	,,		
23	¾	10/11/16	description, useful instructions			
24	**4/4**	12/11/16	Memory Systems, Memory maps	,,	Assignmnt –IV	
25	**5/4**	15/11/16	Memory Systems, Memory maps (contd..)	,,		
26	**6/4**	17/11/16	Cortex M3 implementation overview	,,		
27	**7/4**	19/11/16	pipeline and bus interface	,,		
28	**8/4**	25/11/16	pipeline and bus interface (contd..)	Board, chalk, Duster		
29	**1/5**	27/11/16	**Module –5** Exceptions	,,	Assignment -V	
30	**2/5**	2/12/16	Nested Vector interrupt controller design,	,,		
31	**3/5**	5/12/16	Systick Timer			
32	**4/5**	8/12/16	Cortex-M3 Programming using assembly			
33	**5/5**	9/12/16	Cortex-M3 Programming using assembly and C language			
34	**6/5**	10/12/16	CMSIS	,,		

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Session wise – Course Plan

Department of Electronics and Communication Engineering

SEMESTER :I
BRANCH : ECE
SUBJECT : DSDV
SUBJECT CODE : 16EVE151
NO OF HRS/WK : 4

NAME OF THE FACULTY : Mr. Sharana Basava
DATE OF COMMENCEMENT : 26.09.2016
DATE OF CLOSING : 20.12.2016
CLASS STRENGTH : 2
TOTAL HRS : 50

S.No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	26/9/16 27/9/16 28/9/16 29/9/16 30/9/16	**module –1** **Introduction and methodology, digital s/ms and embedded s/ms, binary representation and circuit elements, real world circuits,models,design methodology.**	Board, chalk, Duster	Prerequisite	
2	**2/1**	1/10/16 3/10/16 4/10/16 5/10/16 6/10/16 11/10/16	Module 2 Number basics Unsigned and signed integers,fixed and floating point numbers Sequential basics Storage elements,counters,sequential data paths and control,clocked	,,		

			synchronous timing methodology			
3	**3/1**	12/10/16 15/10/16 15/10/16 19/10/16 20/10/16 2/11/16 3/11/16	Module 3 Memories: Concepts ,memory types,error detection and correction Implementation fabrics ICs,PLDs,packaging and circuit boards,interconnection and signal integrity	,,		
4	**4/1**	5/11/16 6/11/16 11/11/16 12/11/16 15/11/16 17/11/16 19/11/16 25/11/16	Module4 Processor basics: Embedded computer organization,instruction and data,interfacing with memory I/O interfacing: I/O devices,I/O controllers,parallel buses,serial transmission,I/O software.	,,	Assignment - I	
5	**5/1**	25/11/16 2/12/16 5/12/16 8/12/16 9/12/16 10/12/16	Module5 Accelerators:concepts,case study,verification of accelerators. Design methodology: Design flow,design optimization,design for test	,,		
6	**6/1**	30/9/16		,,		

7	**½**	1/10/16	**module –2**			
8	**2/2**	3/10/16		,,		
9	**3/2**	4/10/16		Board, chalk, Duster		
10	**4/2**	5/10/16		,,	Assignment -II	
11	**5/2**	6/10/16		,,		
12	**6/2**	11/10/16		,,		
13	**1/3**	12/10/16	**Module –3**	,,		
15	**2/3**	15/10/16				
16	**3/3**	15/10/16		,,		
17	**4/3**	19/10/16		Board, chalk, Duster		
18	**5/3**	20/10/16		,,	Assignment –III	
19	**6/3**	2/11/16		,,		
20	**7/3**	3/11/16		,,		
21	**¼**	5/11/16	**MODULE –4**	,,		
22	**2/4**	6/11/16		,,		
23	**¾**	10/11/16				
24	**4/4**	12/11/16		,,	Assignmnt –IV	
25	**5/4**	15/11/16		,,		
26	**6/4**	17/11/16		,,		
27	**7/4**	19/11/16		,,		
28	**8/4**	25/11/16		Board, chalk, Duster		

29	**1/5**	27/11/16	**Module –5**	,,	Assignment -V	
30	**2/5**	2/12/16		,,		
31	**3/5**	5/12/16				
32	**4/5**	8/12/16				
33	**5/5**	9/12/16				
34	**6/5**	10/12/16		,,		

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Session wise – Course Plan

Department of Electronics and Communication Engineering

SEMESTER :I
BRANCH : ECE
SUBJECT : DVD
SUBJECT CODE : 16EVE12
NO OF HRS/WK : 4

NAME OF THE FACULTY : Dr. Ramesh
DATE OF COMMENCEMENT : 26.09.2016
DATE OF CLOSING : 20.12.2016
CLASS STRENGTH : 7
TOTAL HRS : 50

S.No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	26/9/16	**module –1** **MOS Transistor**: The Metal Oxide Semiconductor (MOS) Structure,	Board, chalk, Duster	Prerequisite	
2	**2/1**	26/9/16	The MOS System under External Bias,	,,		
3	**3/1**	27/9/16	Structure and Operation of MOS Transistor	,,		
4	**4/1**	28/9/16	Structure and Operation of MOS Transistor (contd..)	,,	Assignment - I	
5	**5/1**	29/9/16	MOSFET Current-Voltage Characteristics,	,,		
6	**6/1**	30/9/16	MOSFET Scaling and Small-Geometry Effects.	,,		
7	**7/1**	1/10/16	**MOS Inverters-Static Characteristics**: Introduction, Resistive-Load inverter			
8	**8/1**	3/10/16	Inverters with n_Type MOSFET Load.	,,		

9	**1/2**	4/10/16	**module –2** **MOS Inverters-Static** **Characteristics**: CMOS Inverter.	Board, chalk, Duster		
10	**2/2**	5/10/16	**MOS Inverters**: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition,	,,	Assignment -II	
11	**3/2**	6/10/16	Calculation of Delay Times, Inverter Design with Delay Constraints,	,,		
12	**4/2**	11/10/16	Esimation of Interconnect Parasitics, Calculation of Interconnect Delay	,,		
13	**5/3**	12/10/16	Switching Power Dissipation of CMOS Inverters.	,,		
15	**1/3**	15/10/16	**Module –3** **Semiconductor Memories:** Introduction			
16	**2/3**	15/10/16	Dynamic Random Access Memory (DRAM)	,,		
17	**3/3**	19/10/16	Dynamic Random Access Memory (DRAM) (contd..)	Board, chalk, Duster		
18	**4/3**	20/10/16	Static Random Access Memory (SRAM),	,,	Assignment –III	
19	**5/3**	2/11/16	Nonvolatile Memory	,,		
20	**6/3**	3/11/16	Flash Memory, Ferroelectric Random Access Memory (FRAM).	,,		
21	**¼**	5/11/16	**MODULE –4** **Dynamic Logic Circuits**: Introduction, Basic Principles of Pass Transistor Circuits,	,,		
22	**2/4**	6/11/16	Voltage Bootstrapping,	,,		

			Synchronous Dynamic Circuit Techniques			
23	¾	10/11/16	Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.			
24	**4/4**	12/11/16	**BiCMOS Logic Circuits**: Introduction	,,	Assignmnt –IV	
25	**5/4**	15/11/16	Bipolar Junction Transistor (BJT): Structure and Operation	,,		
26	**6/4**	17/11/16	Dynamic Behavior of BJTs, Basic BiCMOS Circuits	,,		
27	**7/4**	19/11/16	Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.	,,		
28	**8/4**	25/11/16	Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications. (contd..)	Board, chalk, Duster		
29	**1/5**	27/11/16	**Module –5** **Chip Input and Output (I/O) Circuits**: Introduction, ESD Protection, Input Circuits	,,	Assignment -V	
30	**2/5**	2/12/16	Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution	,,		
31	**3/5**	5/12/16	Latch-Up and Its Prevention			
32	**4/5**	8/12/16	**Design for Manufacturability**: Introduction, Process Variations,			
33	**5/5**	9/12/16	Basic Concepts and Definitions,			
34	**6/5**	10/12/16	Design of Experiments and Performance Modeling.	,,		

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Session wise – Course Plan

Department of Electronics and Communication

SEMESTER : I
BRANCH : TCE
SUBJECT : ADM
SUBJECT CODE: 16ELD11
NO OF HRS/WK: 5

NAME OF THE FACULTY : Rajesh Gopal
DATE OF COMMENCEMENT : 15.10/2016
DATE OF CLOSING : 15.12/.2016
CLASS STRENGTH : 08
TOTAL HRS : 52

Session No	Chapter no (No of hrs planed for the module)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/(10 hrs)**	15/10/16 To 30/10/16	**Module 1: Linear Algebra-I, Vector spaces, sub-space, linearly independent vectors, basis vectors, dimension of vector space, linear transformation, rank-nullity theorem, matrix form of linear transformation**	Board, chalk, duster		
2	**2/(10 hrs)**	1/11/16 To 15/11/16	Module2 : Probability Theory Review of basic theory, definition of random variables, probability distribution, probability mass and density function, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions, Binomial, Poisson, Exponential, Gaussian and Rayleigh distribution	,,		
3	**3/(10 hrs)**	16/11/16 To 27/11/16	Module 3-Joint Probability distributions, Properties of CDF, PDF, PMF, conditional distributions, Expectation, covariance and correlation, Independent random variables, Central limit theorem, Random process, Stationary and Ergodic, Auto correlation function, properties, Gaussiam random process			
4	**4 /(10 hrs)**	28/11/16 To	Module 4 : Linear Algebra II, Eigen values and Eigenvectors	,,		

		7/12/16	of real symmetric matrices, Given's method, orthogonal vectors and bases, Gram-Schmidt orthogonalization, QR decomposition, Singular value decomposition, least square approximations.			
5	**5/(10 hrs)**	8/12/16 To 15/12/16	Module 5: Calculus of variations, Concept of functional- Eulers equation, functional dependent on first and higher order derivatives, functional on several dependent variables. Isoperimetric problems- variation problems with moving boundaries	,,		

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Session wise – Course Plan

Department of Electronics and Communication Engineering

SEMESTER :I
BRANCH : ECE
SUBJECT : LPVLSI
SUBJECT CODE : 16EVE14
NO OF HRS/WK : 4

NAME OF THE FACULTY : Mr. Sharanabasappa S H
DATE OF COMMENCEMENT : 26.09.2016
DATE OF CLOSING : 20.12.2016
CLASS STRENGTH : 2
TOTAL HRS : 50

S.No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	**26/9/16**	**module –1** Introduction: Need for low power VLSI chips, Charging and discharging capacitance .	Board, chalk, Duster	Prerequisite	
2	**2/1**	26/9/16	Short circuit current in CMOS leakage current, Static current	,,		
3	**3/1**	27/9/16	Basic principle of low power design	,,		
4	**4/1**	28/9/16	Low power figure of merits	,,	Assignment - I	
5	**5/1**	29/9/16	**Simulation Power analysis**: SPICE circuit simulators, Discrete transistor modelling and analysis.	,,		
6	**6/1**	30/9/16	Gate level logic simulation Architecture level analysis, Data correlation analysis in DSP systems, Monte Carlo simulation	,,		
7	½	1/10/16	**module –2**			

			Probabilistic power analysis: Random logic signals			
8	**2/2**	3/10/16	Probability & frequency Probabilistic power analysis techniques,	,,		
9	**3/2**	4/10/16	Signal entropy	Board, chalk, Duster		
10	**4/2**	5/10/16	**Circuit :**transistor and gate sizing ,equivalent pin ordering,	,,	Assignment -II	
11	**5/2**	6/10/16	Network restructuring and reorganizing, special latches and flip_flops	,,		
12	**6/2**	11/10/16	Low power digital cell library, adjustable device threshold voltage	,,		
13	**1/3**	12/10/16	**Module –3** **Logic level:** Gate reorganization, Signal gating, logic encoding	,,		
15	**2/3**	15/10/16	State machine encoding Pre-computation logic			
16	**3/3**	15/10/16	**Low power clock distribution:** Power dissipation in clock distribution	,,		
17	**4/3**	19/10/16	Single driver vs distributed buffers	Board, chalk, Duster		
18	**5/3**	20/10/16	Zero skew vs tolerable skew	,,	Assignment –III	
19	**6/3**	2/11/16	Chip package and package codesign of clock level	,,		
				,,		
21	**¼**	5/11/16	**MODULE –4**	,,		

			Low power Architecture & Systems: Power & performance management,			
22	**2/4**	6/11/16	Power and performance management,Switching activity reduction	,,		
23	¾	10/11/16	Parallel architecture with voltage reduction Flow graph transformation,			
24	**4/4**	12/11/16	**Low power arithmetic components**	,,	Assignmnt –IV	
25	**5/4**	15/11/16	Introduction	,,		
26	**6/4**	17/11/16	Circuit design style	,,		
27	**7/4**	19/11/16	Adders ,multipliers	,,		
28	**8/4**	25/11/16	division	Board, chalk, Duster		
29	**1/5**	27/11/16	**Module –5** Low power memory design. Introduction , source and reduction of power dissipation in memory subsystem	,,	Assignment -V	
30	**2/5**	2/12/16	Sources and power dessipation in DRAM and SRAM	,,		
31	**3/5**	5/12/16	**s**			
32	**4/5**	8/12/16	Algorithmic level analysis & optimization, Architectural level estimation & synthesis			
33	**5/5**	9/12/16	**Advanced technique :** adiabatic computation .			
34	**6/5**	10/12/16	Pass transistors,asyncronous circuits.	,,		

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