#132, AECS Layout, IT Park Road, Kundalahalli, Bangalore – 560 037
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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication

SEMESTER :V
BRANCH :ECE(D)
SUBJECT :Digital Signal Processing
SUBJECT CODE :15EC52
NO OF HRS/WK:6

NAME OF THE FACULTY: Mr.Raveesh Hegde
DATE OF COMMENCEMENT: 25.07.2016
DATE OF CLOSING: 19.11.2016
CLASS STRENGTH: 65
TOTAL HRS: 64

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	1/0	07.08.17	Review of Signals and Systems	Board, chalk, duster	A1	
2	2/0	08.08.17	Periodicity of sinusoids	,,		
3	3/0	09.08.17	Properties of systems	,,		
4	4/0	10.08.17	Convolution	,,		
5	5/0	11.08.17	Problems on convolution	,,		
6	6/0	12.08.17	Complex exponential as Eigen Function of LTI systems.	,,		
7	7/0	14.08.17	Introduction to Fourier Representation of Signals	,,		

8	8/0	16.08.17	A problem on Fourier Series, discussion on nature of the spectrum	,,		
9	9/0	17.08.17	Trigonometric Fourier Series	,,		
10	10/0	18.08.17	Properties of Fourier series, Dirichlet Conditions, Parsevals theorem.	,,		
11	11/0	19.08.17	Introduction to Fourier Transform. 1 problem.	,,		
12	12/0	21.08.17	Problems on Fourier Transform, Dirac delta function.	,,		
13	13/0	23.08.17	Problems on FT	,,		
14	14/0	24.08.17	DTFS	,,		
15	15/0	28.08.17	Problems on DTFS, Discussion on DTFT	,,		
16	1/1	30.08.17	Frequency domain sampling, DFT	,,	A2	
17	2/1	31.08.17	DFT and some properties, magnitude and phase spectrum.	,,		
18	3/1	01.09.17	Problems on DFT	,,		
19	4/1	04.09.17	DFT as linear transformation, some problems.	,,		
20	5/1	05.09.17	Recap of DFT as linear transformation, properties of Wn, relationship of DFT to DTFS.	,,		
21	6/1	06.09.17	Relationship between DFT and Z transform, DFT and CTFS coefficients, DFT and DTFT	,,		
22	7/1	07.09.17	Parsevals theorem, Circular symmetry of a sequence	,,		

23	8/1	08.09.17	Circular Symmetries of a sequence	,,		
24	9/1	09.09.17	Circular Convolution, derivation, problem solving methods	,,		
25	1/2	11.09.17	Additional properties of DFT	,,	A3	
26	2/2	12.09.17	Correlation, parsevals theorem, linear convolution using circular convolution.	,,		
27	3/2	13.09.17	Filtering of long data sequences, overlap add method	,,		
28	4/2	14.09.17	Overlap save method, problem	,,		
29	5/2	15.09.17	Introduction to FFT algorithms	,,		
30	1/3	22.09.17	Radix 2 DIT FFT algorithm	,,	A4	
31	2/3	23.09.17	Problems on DIT FFT algorithm	,,		
32	3/3	25.09.17	Problems on DIT FFT algorithm	,,		
33	4/3	26.09.17	Problems on DIT FFT algorithm	,,		
34	5/3	27.09.17	Computational complexity of DIT FFT, Derivation of DIF FFT	,,		
35	6/3	28.09.17	Problems on DIF FFT	,,		
36	7/3	03.10.17	Problems on DIF FFT	,,		
37	8/3	04.10.17	DIT -IFFT, Goertzel algorithm	,,		
38	9/3	06.10.17	Chirp Z transform	,,		

39	10/3	07.10.17	DFT of 2 real sequences, DFT of 2N point sequence.	,,		
40	1/4	09.10.17	Impulse response of ideal filters.	,,	A5	
41	2/4	10.10.17	Basics of filter design, impulse response from even and odd parts.	,,		
42	3/4	11.10.17	relationship between real and imaginary parts of frequency response, types of filters	,,		
43	4/4	12.10.17	FIR filters, linear phase, different types of FIR filters	,,		
44	5/4	13.10.17	Different types of FIR filters, z transforms and frequency response	,,		
45	6/4	14.10.17	FIR filter design using windows	,,		
46	7/4	16.10.17	Problems on FIR filter design	,,		
47	8/4	17.10.17	Problems on FIR filter design	,,		
48	9/4	23.10.17	FIR Filter Design using Kaiser window	,,		
49	10/4	24.10.17	FIR Filter Design using Kaiser window	,,		
50	1/5	25.10.17	IIR filter design, Laplace transform, z transform	,,	A6	
51	2/5	26.10.17	Introduction to IIR filter design from analog filters	,,		
52	3/5	27.10.17	Properties of mapping functions. Introduction to IIR filter design using impulse invariance method	,,		
53	4/5	28.10.17	IIR filter design by approximation of derivatives	,,		

54	5/5	30.10.17	Approximation of derivatives, problems	,,		
55	6/5	31.10.17	Bilinear Transformation	,,		
56	7/5	02.11.17	Problems on Bilinear Transformation	,,		
57	8/5	03.11.17	Problems on bilinear transformation, matched z transform	,,		
58	9/5	04.11.17	Butterworth filter design- derivations	,,		
59	10/5	09.11.17	Problems on butterworth filter design	,,		
60	11/5	10.11.17	Analog frequency transformations	,,		
61	12/5	13.11.17	Chebyshev Filter Design	,,		
62	13/5	14.11.17	Chebyshev Filter Design problems	,,		
63	14/5	15.11.17	Direct form I and II realization of systems. Parallel Form, Cascade Form,	,,	A7	
64	15/5	16.11.17	Linear Phase FIR structures, Lattice structure realization of filters.	,,		

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INSTITUTE OF

TECHNOLOGY

Lesson Plan

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SEM : V

NAME OF THE FACULTY : Harsha B. K.

Rahul N.

Shruthi M. L. J.

BRANCH : ECE

DATE OF COMMENCEMENT : 07.08.2017

SUBJECT : ITC

DATE OF CLOSING : 15.11.2017

SUBJECT CODE : 15EC54

CLASS STRENGTH : 60

NO OF HRS/WK : 5

TOTAL HRS : 55

No	Chapter no (No of hrs planed for the chapter)	Date	Topics planned for the session	Teaching Aids	Assignments/Tests planned for the chapter	Topics covered As per plan
1	-	07-08	Model of communication system, Introduction to Probabilities, Joint probabilities,	Board, chalk, duster		
2	-	08-08	Probability distribution function, Random variables,	"-"		

			Discrete random variables,			
3	-	09-08	Continuous random variables, Random process, Noise in communication system Perquisite	"-"		
4	1/1	**10-08**	**Information theory:** Introduction, Measure of information,.	"-"	Assignment 1	
5	2/1	11-08	Average information content of symbols in long independent sequences	"-"		
6	3/1	14-08	Problems on information content, Calculation of entropy.	"-"		
7	4/1	16-08	Information rate, average information rate. Numerical calculations.	"-"		
8	5/1	17-08	Average information content of symbols in long dependent sequences.	"-"		
9	6/1	18-08	Numerical	"-"		
10	7/1	19-08	Markov statistical model for information source.	"-"		
11	8/1	22-08	Entropy and Information rate of markov source.	"-"		
12	9/1	23-08	Problems on markov sources. Key points.	"-"		
13	10/1	24-08	Revision and class test on Module-1	"-"		
14	1/2	**28-08**	**Source Coding:** Introduction to encoding the source output. Source coding theorem.	"-"	Assignment 2	
15	2/2	29-08	Prefix Codes Kraft McMillan Inequality Property	"-"		

16	3/2	31-08	Encoding of the Source Output, Shannon's Encoding Algorithm	"-"		
17	4/2	01-09	Shannon Fano Encoding Algorithm	"-"		
18	5/2	04-09	Huffman codes	"-"		
19	6/2	05-09	Numerical on Huffman codes	"-"		
20	7/2	06-09	Extended Huffman coding	"-"		
21	8/2	08-09	Arithmetic Coding	"-"		
22	9/2	09-09	Lempel – Ziv Algorithm	"-"		
23	10/2	11-09	Revision and class test on Module-2	"-"		
24	1/3	**12-09**	**Information Channels:** Communication Channels	"-"	Assignment 3	
25	2/3	13-09	Channel Models,	"-"		
26	3/3	15-09	Channel Matrix, Joint probability Matrix	"-"		
27	4/3	22-09	Binary Symmetric Channel,	"-"		
28	5/3	23-09	System Entropies, Mutual Information, Channel Capacity	"-"		
29	6/3	25-09	Channel Capacity of : Binary Symmetric Channel	"-"		
30	7/3	26-09	Binary Erasure Channel	"-"		
31	8/3	28-09	Muroga's Theorem	"-"		
32	9/3	03-10	Continuous channels	"-"		
33	10/3	04-10	Revision and class test on Module-3	"-"		
34	1/4	**06-10**	**Introduction to Error Control Coding:**	"-"		

			Examples of error control coding.			
35	2/4	07-10	Methods of Controlling Errors, Types of Errors, types of Codes.	"-"		
36	3/4	10-10	Linear Block Codes Matrix description	"-"		
37	4/4	11-10	Error detection and correction,	"-"		
38	5/4	12-10	Single Error Correcting hamming Codes	"-"		
39	6/4	13-10	Standard arrays and table look up for decoding. Numerical	"-"		
40	7/4	14-10	Algebraic Structure of Cyclic Codes	"-"		
41	8/4	17-10	Encoding using an (n-k) Bit Shift register, Syndrome Calculation	"-"		
42	9/4	23-10	Error Detection and Correction	"-"		
43	10/4	24-10	Revision and class test on Module-4	"-"		
44	1/5	**25-10**	**Cyclic Codes:** Golay Codes	"-"		
45	2/5	26-10	BCH Codes	"-"		
46	3/5	28-10	**Convolution Codes:** Introduction, Time domain approach	"-"		
47	4/5	30-10	Transform domain approach	"-"		
48	6/5	31-10	State table, state transition table.	"-"		
49	7/5	02-11	Trellis and State diagram. Code tree	"-"		
50	8/5	03-11	The Viterbi Algorithm	"-"		
51	9/5	09-11	Numerical and revision of Module-5	"-"		

52	10/5	10-11	Class test on Module-5	"-"	Assignment 5	
53		**13-11**	Revision	"-"		
54		14-11	Revision	"-"		
55		15-11	Revision	"-"		

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of ECE

SEMESTER : V NAME OF THE FACULTY : Mr. Nitin Salunkhe

BRANCH : ECE DATE OF COMMENCEMENT : 08-08-2017

SUBJECT : MANAGEMENT & ENTREPRENEURSHIP DATE OF CLOSING : 15-11-2017

SUBJECT CODE: 15EC51 CLASS STRENGTH : 55

NO OF HRS/WK: 15 TOTAL HRS : 50 Hours

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per

						plan
1	**1/1**	08/08/2017	**Module 1:** Introduction to Management	Board, chalk, duster		
2	**1/2**	08/08/2017	Meaning & Definition of Management	,,		
3	**1/3**	09/08/2017	Nature & Characteristics of Management (Management as an art, science & profession)	,,		
4	**1/4**	10/08/2017	Importance of Management	,,		
5	**1/5**	11/08/2017	Management & Administration	,,		
6	**1/6**	12/08/2017	Roles & Levels of Management	,,		
7	**1/7**	14/08/2017	Functions of Management	CASE STUDY		
8	**1/8**	16/08/2017	Planning: Nature, Importance & Purpose	Board, chalk, duster		
9	**1/9**	17/08/2017	Planning Process & Types of Plans	,,		
10	**1/10**	18/08/2017	Decision Making & Steps in decision making	,,		
11	**1/11**	19/08/2017	Recapitulation of Module 1		Assignment 1	
12	**2/1**	21/08/2017	Module 2: Nature & Purpose of organizing	,,		
13	**2/2**	22/08/2017	Principles & Types of organization	,,		
14	**2/3**	23/08/2017	Span of control-MBO & MBE	,,		

	2/4	24/08/2017	Staffing-Selection & Recruitment	,,		
15	**2/5**	28/08/2017	Meaning & Nature of Directing	,,		
16	**2/6**	29/08/2017	Leadership Styles	CASE STUDY		
17	**2/7**	30/08/2017	Motivation Theories	PPT		
18	**2/8**	31/08/2017	Communication-Meaning & Importance	Board, chalk, duster		
19	**2/9**	01/09/2017	Coordination-Meaning, Importance & Techniques	,,		
20	**2/10**	04/09/2017	Meaning & Steps in controlling	,,		
21	**2/11**	05/09/2017	Recapitulation of Module 2		Assignment 2	
22	**3/1**	06/09/2017	Module 3: Meaning of Social Responsibility	PPT		
23	**3/2**	07/09/2017	Responsibility Towards different groups	,,		
24	**3/3**	08/09/2017	Social Audit , Business Ethics	,,		
25	**3/4**	09/09/2017	Corporate Governance	CASE STUDY		
26	**3/5**	11/09/2017	Entrepreneurship- Meaning & Evolution of concept & Importance	Board, chalk, duster		
27	**3/6**	12/09/2017	Characteristics of successful entrepreneurs	Quiz		
28	**3/7**	13/09/2017	Classification for Entrepreneurs, Intra-preneur	Board, chalk, duster		

29	**3/8**	14/09/2017	Myths of Entrepreneurship & Entrepreneurial Development Models	,,		
30	**3/9**	15/09/2017	Problems faced by Entrepreneurs and capacity building for Entrepreneurship	,,		
31	**3/10**	22/09/2017	Recapitulation of Module 1	,,		
32	**3/11**	23/09/2017	Recapitulation of Module 2	,,		
33	**4/1**	25/09/2017	Module 4: Role of Small Scale Industries	,,		
34	**4/2**	26/09/2017	Concepts and definitions of SSI Enterprises	,,		
35	**4/3**	03/10/2017	Government policy and development of the Small Scale sector in India	Board, chalk, duster		
36	**4/4**	04/10/2017	Growth and Performance of Small Scale Industries in India	PPT		
37	**4/5**	06/10/2017	Sickness in SSI sector, Problems for Small Scale Industries	Board, chalk, duster		
38	**4/6**	07/10/2017	Impact of Globalization on SSI	,,		
39	**4/7**	09/10/2017	Impact of WTO/GATT on SSIs, Ancillary Industry and Tiny Industry	GD		
40	**4/8**	10/10/2017	Institutional Support for Business Enterprises	Board, chalk, duster		
41	**4/9**	11/10/2017	Schemes of Central–Level Institutions, State-Level	"	Assignment-3	

			Institutions			
42	**4/10**	12/10/2017	Recapitulation of Module 4			
43	**5/1**	13/10/2017	Module5: Meaning of Project, Project Objectives & Characteristics	,,		
44	**5/2**	14/10/2017	Project Identification- Meaning & Importance	,,		
45	**5/3**	16/10/2017	Project Life Cycle, Project Scheduling	,,		
46	**5/4**	17/10/2017	Capital Budgeting, Generating an Investment Project Proposal	,,		
47	**5/5**	23/10/2017	Project Report-Need and Significance of Report, Contents, Formulation	,,		
48	**5/6**	24/10/2017	Project Analysis-Market, Technical, Financial, Economic, Ecological, Project Evaluation and Selection	CASE STUDY		
49	**5/7**	25/10/2017	Project Financing, Project Implementation Phase	Board, chalk, duster		
50	**5/8**	26/10/2017	Human & Administrative aspects of Project Management, Prerequisites for Successful Project Implementation	,,		
51	**5/9**	27/10/2017	New Control Techniques- PERT	,,		

			and CPM			
52	**5/10**	28/10/2017	Steps involved in developing the network	,,		
53	**5/11**	30/10/2017	Uses and Limitations of PERT and CPM	,,		
54		31/10/2017	Recapitulation of Module 5			
55		02/11/2017	Discussion of VTU Questions			
56		03/11/2017	REVISION			
57		04/11/2017	REVISION			

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Session wise – Course Plan

Department of Electronics and Communication Engineering

SEMESTER : V **NAME OF THE FACULTY : Priyanka R**

BRANCH : ECE **DATE OF COMMENCEMENT : 7/8/17**

SUBJECT :Operating System **DATE OF CLOSING : 25/11/17**

SUBJECT CODE : 15EC553 **CLASS STRENGTH :**

NO OF HRS/WK : 5 **TOTAL HRS : 55**

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	7.8.17	Briefing the syllabus, Mode of class and study, Prerequisites of the course, Expectation from the student.	Chalk & Talk		

2	**2/1**	8.8.17	**UNIT 1 INTRODUCTION AND OVERVIEW OF OPERATING SYSTEMS:** Introduction about O.S	,,		
3	**3/1**	9.8.17	Goals of an OS, Operation of an OS,	,,		
4	**4/1**	12.8.17	Computational Structures, Resource allocation techniques,,	,,		
5	**5/1**	12.8.17	Efficiency, System Performance and User Convenience,	,,	Assignment-I	
6	**6/1**	14.8.17	Classes operating System,	,,		
7	**7/1**	16.8.17	Batch processing,	,,		
8	**8/1**	17.8.17	Batch processing continued ..	,,		
9	**9/1**	21.8.17	Time Sharing Systems			
10	**10/1**	22.8.17	Real Time systems			
11	**11/1**	23.8.17	distributed Operating Systems			
12	**12/1**	24.8.17	distributed Operating Systems continued…			
13	**13/1**	30.8.17	**Test on UNIT 1**	,,		
14	**1/2**	30.8.17	**Unit 2:Process Management:** OS View of Processes	,,		

15	**2/2**	31.8.17	PCB	,,		
16	**3/2**	1.9.17	Fundamental State Transitions,	,,		
17	**4/2**	1.9.17	Threads,	,,		
18	**5/2**	4.9.17	Kernel and User level Threads,	,,		
19	**6/2**	7.9.17	Non-preemptive scheduling- FCFS	,,	Assignment II	
20	**7/2**	7.9.17	SRN	,,		
21	**8/2**	8.9.17	Preemptive Scheduling- RR and LCN			
22	**9/2**	9.9.17	Long term medium term short term scheduling in a time sharing system			
23	**10/2**	11.9.17	**Test on UNIT 2**	,,		
24	**1/3**	14.9.17	**Unit 3:Memory Management:** Contiguous Memory allocation,	,,		
25	**2/3**	14.9.17	Non-Contiguos Memory	,,		

			Allocation,			
26	**3/3**	15.9.17	Non-Contiguos Memory Allocation continued	,,		
27	**4/3**	22.9.17	Paging,	,,		
28	**5/3**	23.9.17	Paging continued..	,,		
29	**6/3**	27.9.17	Segmentation	,,		
30	**7/3**	28.9.17	Segmentation continued			
31	**8/3**	3.10.17	Segmentation with paging,			
32	**9/3**	4.10.17	Segmentation with paging continued…	,,		
33	**10/3**	9.10.17	Virtual Memory Management,			
34	**11/3**	10.10.17	Virtual Memory Management continued…	,,	Assignment III	
35	**12/3**	11.10.17	Demand Paging,	,,		
36	**13/3**	12.10.17	Demand Paging continued…	,,		
37	**14/3**	16.10.17	VM handler FIFO LRU page	,,		

			replacement policies			
38	**1/4**	17.10.17	**Unit 4 File Systems:** File systems and IOCS	,,		
39	**2/4**	23.10.17	File Operations	,,	Assignment IV	
40	**3/4**	27.10.17	File Organizations,	,,		
41	**4/4**	28.10.17	Directory structures,	,,		
42	**5/4**	30.10.17	File Protection,	,,		
43	**6/4**	31.10.17	Allocation of disk space,	‘’		
44	**7/4**	4.11.17	Implementing file access			
45	**8/4**	4.11.17	Interface between File system and IOCS,			
46	**1/5**	9.11.17	**Message Passing and Deadlocks**: Overview of Message Passing,	,,		
47	**2/5**	10.11.17	Implementing message passing, Mailboxes,	,,		

48	**3/5**	11.11.17	Deadlocks in resource allocation, Resource	,,	Assignment V	
49	**4/5**	12.11.17	state modelling, Deadlock detection algorithm	,,		
50	**5/5**	13.11.17	Deadlock Prevention	,,		
51	**6/5**	14.11.17	Deadlocks in resource allocation, Resource	,,		
52	**7/5**	15.11.17	Deadlock detection algorithm	,,		
53	**8/5**	16.11.17	Deadlock Prevention	,,	Assignment VI	
55	**9/5**	16.11.17	Deadlock Prevention continued…	,,		

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OF TECHNOLOGY

Session wise – Course Plan

SEMESTER/SECTION:	5	NAME OF THE FACULTY:	SUNIL KUMAR K H
BRANCH :	ECE	DATE OF COMMENCEMENT:	07/08/2017
SUBJECT :	Verilog HDL	DATE OF CLOSING:	16/11/2017
SUBJECT CODE :	15EC53	CLASS STRENGTH:	62(C sec)/65(D sec)
NO OF HRS/WEEK :	5	TOTAL HRS:	55

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Testsplanned for the chapter	Topics covered As per plan

1	**Prerequisites**	**07/08/2017**	Logic Design	Board, Chalk, Duster		
2		**07/08/2017**	Logic Design	Board, Chalk, Duster	Assignment – 1	
3	**Module 1 (8 Hours)**	**10/08/2017**	**Overview of Digital Design with Verilog HDL:** Evolution of CAD, Emergence of HDLs	Board, Chalk, Duster		
4		**11/08/2017**	Typical HDL-flow	Board, Chalk, Duster		
5		**11/08/2017**	Why Verilog HDL?	Board, Chalk, Duster		
6		**14/08/2017**	Trends in HDLs	Board, Chalk, Duster		
7		**14/08/2017**	**Hierarchical Modeling Concepts:** Top-down and bottom-up design methodology	Board, Chalk, Duster	Assignment – 2	
8		**18/08/2017**	Differences between modules and Module instances	Board, Chalk, Duster		
9		**19/08/2017**	Parts of a simulation	Board, Chalk, Duster		
10		**19/08/2017**	Design block, Stimulus block	Board, Chalk, Duster		
11	**Module 2 (9 Hours)**	**22/08/2017**	**Basic Concepts:** Lexical conventions	Board, Chalk, Duster		

12		**22/08/2017**	Data types	Board, Chalk, Duster		
13		**28/08/2017**	Data types(contd.)	Board, Chalk, Duster		
14		**29/08/2017**	System tasks, Compiler directives	Board, Chalk, Duster	Assignment – 3	
15		**29/08/2017**	**Modules and Ports:** Module definition, port declaration	Board, Chalk, Duster		
16		**31/08/2017**	Connecting ports	Board, Chalk, Duster		
17		**31/08/2017**	Hierarchical name referencing	Board, Chalk, Duster		
18		**05/09/2017**	Revision	Board, Chalk, Duster		
19		**06/09/2017**	Unit Test-1	-		
20	**Module 3** **(9 Hours)**	**06/09/2017**	**Gate-Level Modeling:** Modeling using basic Verilog gate primitives	Board, Chalk, Duster		
21		**08/09/2017**	Description of and/or and buf/not type gates	Board, Chalk, Duster		
22		**08/09/2017**	Rise, Fall delays	Board, Chalk, Duster		
23		**12/09/2017**	Turn-off delays	Board, Chalk,	Assignment – 4	

				Duster		
24		**13/09/2017**	Min, Max, and Typical delays	Board, Chalk, Duster		
25		**13/09/2017**	**Dataflow Modeling:** Continuous assignments	Board, Chalk, Duster		
26		**15/09/2017**	Delay specification expressions	Board, Chalk, Duster		
27		**15/09/2017**	Operators, Operands	Board, Chalk, Duster	Assignment – 5	
28		**25/09/2017**	Operator types	Board, Chalk, Duster		
29	**Module 4** **(12 Hours)**	**26/09/2017**	**Behavioral Modeling:** Structured procedures	Board, Chalk, Duster		
30		**26/09/2017**	Initial and Always Statements	Board, Chalk, Duster		
31		**28/09/2017**	Blocking statements, Non-Blocking statements	Board, Chalk, Duster		
32		**28/09/2017**	Delay control statements	Board, Chalk, Duster		
33		**06/10/2017**	Generate statement, Event control statements	Board, Chalk, Duster	Assignment – 6	
34		**07/10/2017**	Conditional statements, Multiway branching	Board, Chalk,		

				Duster		
35		**07/10/2017**	Loop statements	Board, Chalk, Duster		
36		**10/10/2017**	Sequential and parallel blocks	Board, Chalk, Duster		
37		**10/10/2017**	Example programs	Board, Chalk, Duster		
38		**13/10/2017**	Example programs	Board, Chalk, Duster		
39		**14/10/2017**	Revision	Board, Chalk, Duster		
40		**14/10/2017**	Unit Test-2	-		
41	**Module 5** **(15 Hours)**	**17/10/2017**	**Introduction to VHDL** **Introduction:** Why use VHDL?	Board, Chalk, Duster		
42		**17/10/2017**	Shortcomings	Board, Chalk, Duster		
43		**25/10/2017**	Using VHDL for Design Synthesis	Board, Chalk, Duster	Assignment – 7	
44		**26/10/2017**	Design tool flow	Board, Chalk, Duster		
45		**26/10/2017**	Font conventions	Board, Chalk, Duster		
46		**28/10/2017**	**Entities and Architectures:**	Board,		

			Introduction, A simple design,	Chalk, Duster		
47		**28/10/2017**	Design Entities	Board, Chalk, Duster		
48		**02/11/2017**	Design Entities (Contd.)	Board, Chalk, Duster		
49		**03/11/2017**	Identifier	Board, Chalk, Duster		
50		**03/11/2017**	Data objects	Board, Chalk, Duster	Assignment – 8	
51		**09/11/2017**	Data types	Board, Chalk, Duster		
52		**09/11/2017**	Data types(Contd.)	Board, Chalk, Duster		
53		**14/11/2017**	Attributes.	Board, Chalk, Duster		
54		**15/11/2017**	Revision	Board, Chalk, Duster		
55		**15/11/2017**	Unit test – 3	-		

Signature of faculty Signature of HOD