#132, AECS Layout, IT Park Road, Kundalahalli, Bangalore – 560 037
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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication

SEMESTER : VII
BRANCH : ECE
SUBJECT : CCN
SUBJECT CODE : 10EC71
NO OF HRS/WK: 5

NAME OF THE FACULTY : JYOTI.M.R /EISHA AKANKSHA
DATE OF COMMENCEMENT : 16.07/2017
DATE OF CLOSING : 9.11.2017
CLASS STRENGTH : 62
TOTAL HRS : 52

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1.	**UNIT-1 Introduction to computer network**	**16/8**	Introduction, Layered tasks, OSI Model	Board, chalk, duster		
2.		**17/8**	TCP/IP suite,	,,		
3.		**18/8**	Addressing	,,		
4.		**19/8**	Telephone and cable networks for data transmission			
5.		**21/8**	Telephone network			
6.		**22/8**	Dial up modem			
7.		**23/8**	DSL			
8.		**24/8**	Cable TV for data transmission			
9.	**UNIT-2 Data link control**	**28/8**	Introduction, Framing			

10		**29/8**	Flow and error control			
11		**30/8**	Protocols			
12		**31/8**	Noiseless channels			
13		**1/9**	Noisy channel			
14		**4/9**	HDLC			
15	**UNIT-3 Multiple access**	**5/9**	Introduction, CSMA			
16		**6/9**	CSMA/CD			
17		**7/9**	ALOHA			
18		**8/9**	Random access			
19		**9/9**	Controlled access			
20		**11/9**	Channelization			
21		**12/9**	TDMA, FDMA, CDMA			
22	**UNIT-4 Wired LAN**	**13/9**	Introduction, Ethernet			
23		**14/9**	IEEE standards			
24		**15/9**	Standard Ethernet			
25		**22/9**	Changes in the standards			
26		**23/9**	Fast Ethernet			
27		**25/9**	Giga bit Ethernet			
28		**26/9**	Wireless LAN			
29		**27/9**	IEEE 802.11			
30	**UNIT-5 Connecting LAN**	**28/9**	Introduction, HUB, Repeater			

31		**3/10**	Bridges			
32		**4/10**	Routers			
33		**6/10**	Gateways			
34		**7/10**	Backbone networks			
35		**9/10**	Virtual LAN			
36		**10/10**	Membership and configuration			
37		**11/10**	Introduction, Logical addressing			
38	**UNIT-6 Network layer**	**12/10**	Introduction, IPV4			
39		**13/10**	IPV6			
40		**14/10**	Comparison			
41		**16/10**	Transition from IPV4 to IPV6			
42		**17/10**	Tunneling, dual stack			
43	**UNIT-7 Delivery**	**23/10**	Introduction, Forwarding			
44		**24/10**	Unicast routing protocols			
45		**25/10**	Distance vector routing protocol			
46		**26/10**	Link state routing protocol			
47		**27/10**	Multicast routing protocol			
48		**28/10**	Comparison			
49		**30/10**	Numerical problems based on routing			
50	**UNIT-8 Transport layer**	**31/10**	Introduction, Process to process delivery			
51		**2/11**	UDP			
52		**3/11**	TCP			
53		**4/11**	DNS			

54		**9/11**	Resolution			
55		**10/11**	Revision			
56		**11/11**	Revision			
57		**13/11**	Revision			
58		**14/11**	Revision			
59		**15/11**	Revision			
60		**16/11**	Revision			
61						
62						

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication

SEMESTER : VII
BRANCH : TCE
SUBJECT : Image Processing
SUBJECT CODE: 10EC754
NO OF HRS/WK: 5

NAME OF THE FACULTY :Priya. R
DATE OF COMMENCEMENT : 16/08/2017
DATE OF CLOSING : 16.11.2017
CLASS STRENGTH : 66
TOTAL HRS : 54

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	17/08/2017	**Unit 1:** DIGITAL IMAGE FUNDAMENTALS**:** What is Digital Image Processing?	Board, Chalk, Duster		
2	**2/1**	17/08/2017	Fundamental Steps in Digital Image Processing,	"		
3	**3/1**	18/08/2017	Components of an Image processing system,	"	Assignment-1	
4	**4/1**	19/08/2017	Elements of Visual Perception.	"		
5	**5/1**	21/08/2017	Applications	"		
6	**1/2**	22/8/2017	**Unit 2:**Image Sensing and Acquisition	"		
7	**2/2**	24/8/2017	Image Sampling and Quantization	"		
8	**3/2**	24/8/2017	Some Basic Relationships between Pixels	"	Assignment-2	
9	**4/2**	28/08/2017	Linear and Nonlinear Operations	"		

10	**5/2**	29/8/2017	Problems	"		
11	**1/3**	31/8/2017	**Unit 3 :**IMAGE TRANSFORMS: Two-dimensional orthogonal & unitary transforms, properties of unitary transforms,	,,		
12	**2/3**	1/9/2017		Board, Chalk, Duster		
13	**3/3**	3/9/2017		"		
14	**4/3**	3/9/2017	Two dimensional discrete Fourier transform.	"	Assignment-3	
15	**5/3**	4/9/2017		"		
16	**6/3**	5/9/2017		,,		
17	**7/3**	6/9/2017	Question paper problems			
18	**1/4**	8/9/2017	**Unit 4:** Discrete cosine transform, sine transform			
19	**2/4**	11/9/2017				
20	**3/4**	11/9/2017	Hadamard transform			
21	**4/4**	12/9/2017	Haar transform		Assignment-4	
22	**5/4**	13/9/2017	Slant transform			
23	**6/4**	15/9/2017	KL transform.			
24	**7/4**	23/9/2017	Problems			
25	**1/5**	23/9/2017	**Unit 5: IMAGE ENHANCEMENT:** Image Enhancement in Spatial domain, Some Basic Gray Level Trans - formations,.	"		
26	**2/5**	25/9/2017		"	Assignment-5	
27	**3/5**	26/9/2017		"		
28	**4/5**	28/9/2017	Histogram Processing, Enhancement Using Arithmetic/Logic Operations	"		
29	**5/5**	4/10/2017		"		
30	**6/5**	4/10/2017		"		
31	**7/5**	6/10/2017		"		

32	**1/6**	7/10/2017	**Unit 6:**Basics of Spatial Filtering	"		
33	**2/6**	10/10/2017		"		
34	**3/6**	12/10/2017	Image enhancement in the Frequency Domain filters	"		
35	**4/6**	13/10/2017		"		
36	**5/6**	13/10/2017	Smoothing Frequency Domain filters	"		
37	**6/6**	14/10/2017	Sharpening Frequency Domain filters	"	Assignment-6	
38	**7/6**	17/10/2017	homomorphic filtering, problems	"		
39	**1/8**	24/10/2017	Unit 8:Color Fundamentals.,	"		
40	**2/8**	24/10/2017	Color Models	"		
41	**3/8**	25/10/2017	., Pseudo color Image Processing	"		
42	**4/8**	26/10/2017	processing basics of full color image processing	"	Assignment-7	
43	**5/8**	28/10/2017		"		
44	**6/8**	31/10/2017		"		
45	**7/8**	31/10/2017	Problems & Question paper revision	"		
46	**1/7**	2/11/2017	**Unit 7:**Model of image degradation/restoration process	"		
47	**2/7**	3/11/2017		"		
48	**3/7**	9/11/2017	noise models	"		
49	**4/7**	11/11/2017	Restoration in the Presence of Noise	Board, Chalk, Duster	Assignment-8	
50	**5/7**	11/11/2017	Only-Spatial Filtering, Periodic Noise Reduction by Frequency Domain Filtering	"		
51	**6/7**	13/11/2017		"		
52	**7/7**	14/11/2017	Linear Position-Invariant Degradations, inverse filtering	"		

53	**8/7**	15/11/2017		“		
54	**9/7**	16/11/2017	minimum mean square error (Weiner) Filtering	“		

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication

SEMESTER : VII
BRANCH : ECE
SUBJECT : DSPA
SUBJECT CODE: 10EC751
NO OF HRS/WK: 5

NAME OF THE FACULTY : Mrs.Reshma P. G.
DATE OF COMMENCEMENT : 16.08.2017
DATE OF CLOSING : 25.11.2017
CLASS STRENGTH : 60
TOTAL HRS : 49

Session No	Chapter no (No of hrs planned for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	17/8/2017	Unit 1:Introduction to DSP: A Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences	Board, chalk, duster	Assignment- I	
2	**2/1**	18/8/2017	Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT)	,,		
3	**3/1**	19/8/2017	Linear Time-Invariant Systems, Digital Filters	,,		
4	**4/1**	21/8/2017	Decimation and Interpolation	,,		
5	**5/1**	22/8/2017	Problems	,,		
6	**1/2**	24/8/2017	Unit 2:Architecture to Programmable DSP processors- Introduction, Basic Architectural Features, DSP Computational Building Blocks-Parallel Multiplier.	,,		

7	**2/2**	28/8/2017	DSP Computational Building Blocks-Shifter, MAC unit	,,		
8	**3/2**	29/8/2017	DSP Computational Building Blocks-ALU	,,		
9	**4/2**	30/8/2017	Bus Architecture and Memory	,,		
10	**5/2**	31/8/2017	Data Addressing Capabilities, Problems	,,		
11	**6/2**	4/9/2017	Data Addressing Capabilities-Specialized Addressing modes	,,	Assignment -II	
12	**7/2**	5/9/2017	Programmability and Program Execution	,,		
13	**8/2**	6/9/2017	Speed Issues-Hardware Architecture, Parallelism, Pipelining	Board, chalk, duster		
14	**9/2**	7/9/2017	System level parallelism and pipelining	,,		
15	**10/2**	8/9/2017	Features for External Interfacing	,,		
16	**1/3**	11/9/2017	Unit 3-Programmable DSP processors :Introduction, Commercial Digital Signal-Processing	,,		
17	**2/3**	12/9/2017	Data Addressing Modes of TMS320C54xx-Bus structure, CPU	,,		
18	**3/3**	13/9/2017	Data Addressing Modes of TMS320C54xx-Immediate, Absolute, Accumulator, Direct Addressing	,,		
19	**4/3**	14/9/2017	Data Addressing Modes of TMS320C54xx- Memory-mapped, Stack Addressing	,,	Assignment –III	
20	**5/3**	15/9/2017	Circular Addressing, Problems for Addressing modes	,,		
21	**6/3**	23/9/2017	Stack Addressing, Indirect, Problems for Addressing modes	,,		
22	**7/3**	25/9/2017	Problems for Addressing modes	,,		
23	**8/3**	26/9/2017	Memory Space of TMS320C54xx Processors	,,		
24	**9/3**	27/9/2017	Program Control, Problems	,,		
25	**1/4**	28/9/2017	Unit 4:Detail Study of TMS320C54X & 54xx	,,		

			Instructions and Programming			
26	**2/4**	4/10/2017	On-Chip peripherals, Interrupts of TMS320C54XX	,,		
27	**3/4**	6/10/2017	Processors Pipeline Operation of TMS320C54xx Processor	,,		
28	**4/4**	7/10/2017	Problems for Pipelining	,,	Assignment –IV	
29	**1/5**	9/10/2017	Unit 5:Implementation of Basic DSP Algorithms: Introduction, The Q-notation, Problems for Q-notation	Board, chalk, duster		
30	**2/5**	10/10/2017	FIR Filters, Program for FIR Filter	,,		
31	**3/5**	12/10/2017	IIR Filters, Program for IIR Filter	,,		
32	**4/5**	13/10/2017	Interpolation filters, Program	,,		
33	**5/5**	14/10/2017	Decimation Filters, Examples, Program	,,	Assignment –V	
34	**1/6**	16/10/2017	Unit 6:Implementation of FFT Algorithms:Introduction, An FFT Algorithm for DFT Computation,	,,		
35	**2/6**	17/10/2017	Overflow and Scaling, Bit-Reversed Index Generation	,,		
36	**3/6**	24/10/2017	8-Point FFT Program implementation on the TMS32OC54xx	,,		
37	**1/7**	25/10/2017	Unit 7:Interfacing of Memory and I/O peripherals: Introduction, Memory Space Organization	,,		
38	**2/7**	26/10/2017	External Bus Interfacing Signals, Memory Interface,	,,		
39	**3/7**	27/10/2017	Problems for memory interface	,,		
40	**4/7**	28/10/2017	Parallel I/O Interface, Programmed I/O			
41	**5/7**	31/10/2017	Interrupts and I/O			
42	**6/7**	2/10/2017	Direct memory access, Memory design examples			
43	**1/8**	3/11/2017	Unit 8:Interfacing and applications of DSP processors-Introduction,			

			Synchronous Serial Interface			
44	**2/8**	4/11/2017	, A Multichannel buffered serial port (McBSP)	Board, chalk, duster		
45	**3/8**	9/11/2017	A CODEC Interface Circuit	,,		
46	**4/8**	13/11/2017	CODEC-DSP Interface Example A DSP System	,,		
47	**5/8**	14/11/2017	A DSP System, DSP Based Bio-telemetry Receiver'	,,	Assignment –VI	
48	**6/8**	15/11/2017	A Speech Processing System	,,		
49	**7/8**	16/11/2017	An Image Processing System.	,,		

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Telecommunication

Semester : VII
Branch : TCE/ECE
Subject : Embedded System Design
Subject Code : 10EC765 / 10EC74
No Of Hrs/ Wk: 5

Name Of The Faculty : Bhumika Narang
Date Of Commencement : 16.08.2017
Date Of Closing : 25.11.2017
Class Strength : 131
Total Hrs : 60

Session No	Chapter no (No of hrs planed for the chapter)	Date	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered as per plan
1	**1/1**	16-08-17	**Unit1: Introduction to Embedded System**- Introducing Embedded Systems, Philosophy	Board & chalk		
2	**2/1**	18-08-17	Embedded Systems, Embedded System Design	,,	Assignment- I	
3	**3/1**	19-08-17	Development Process	,,		
4	**4/1**	21-08-17	Embedded design life cycle	,,		
5	**1/2**	23-08-17	**Unit 2: The Hardware Side**: An Introduction, The Core Level	,,		
6	**2/2**	23-08-17	Representing Information, Understanding Numbers	,,		
7	**3/2**	28-08-17	Addresses, Instructions	,,		
8	**4/2**	29-08-17	Registers-A First Look, Embedded Systems-A Register View, Register View of a Microprocessor	,,		
9	**5/2**	30-08-17	Embedded Systems-An Instruction Set View	,,	Assignment - II	
10	**6/2**	01-09-17	The Hardware Side: Storage Elements	,,		
11	**7/2**	01-09-17	Finite-State Machines The concepts of State and Time, The State Diagram	,,		
12	**8/2**	05-09-17	Finite State Machines- A Theoretical Model.	,,		

13	**1/3**	06-09-17	**Unit 3: Memories and the Memory Subsystem**: Classifying Memory, A General Memory Interface, ROM Overview	LCD Projector		
14	**2/3**	07-09-17	Static RAM Overview	,,		
15	**3/3**	09-09-17	Dynamic RAM Overview	,,		
16	**4/3**	09-09-17	Chip Organization, Terminology	,,		
17	**5/3**	12-09-17	A Memory Interface in Detail, SRAM Design	,,	Assignment – III	
18	**6/3**	13-09-17	DRAM Design	,,		
19	**7/3**	14-09-17	DRAM Memory Interface	,,		
20	**8/3**	22-09-17	The Memory Map, Memory Subsystem Architecture	,,		
21	**9/3**	22-09-17	Basic Concepts of Caching, Designing a Cache System	,,		
22	**10/3**	25-09-17	Dynamic Memory Allocation.	,,		
23	**1/4**	26-09-17	**Unit 4: Embedded Systems Design and Development** : System Design and Development, Life-cycle Models	Board & chalk		
24	**2/4**	27-09-17	Life-cycle Models	,,		
25	**3/4**	03-10-17	Problem Solving-Five Steps to Design, The Design Process	,,		
26	**4/4**	03-10-17	Identifying the Requirements, Formulating the Requirements Specification	,,		
27	**5/4**	04-10-17	The System Design Specification	,,	Assignmnt – IV	
28	**6/4**	06-10-17	System Specifications versus System Requirements, Partitioning and Decomposing a System	,,		
29	**7/4**	07-10-17	Functional Design	,,		
30	**8/4**	09-10-17	Architectural Design	,,		
31	**9/4**	10-10-17	Functional Model versus Architectural Model, Prototyping	LCD Projector		
32	**10/4**	11-10-17	Other Considerations, Archiving the Project.	,,		
33	**1/5&6**	11-10-17	**Unit 5 & 6: Real-Time Kernels and Operating Systems**: Tasks and Things, Programs and Processes	LCD Projector		
34	**2/5&6**	12-10-17	The CPU is a resource	,,		

35	**3/5&6**	13-10-17	Threads – Lightweight and heavyweight	,,	Assignment - V	
36	**4/5&6**	14-10-17	Sharing Resources, Foreground/ Background Systems	,,		
37	**5/5&6**	16-10-17	The operating System, The real time operating system (RTOS)	,,		
38	**6/5&6**	23-10-17	OS architecture	,,		
39	**7/5&6**	23-10-17	Tasks and Task control blocks	,,	Assignment - VI	
40	**8/5&6**	24-10-17	Tasks and Task control blocks	,,		
41	**9/5&6**	25-10-17	Memory management revisited	,,		
42	**10/5&6**	26-10-17	Memory management revisited	,,		
43	**1/7&8**	27-10-17	**Unit 7 & 8: Performance Analysis and Optimization**: Performance or Efficiency Measures, Complexity Analysis	,,		
44	**2/7&8**	28-10-17	The methodology	,,		
45	**3/7&8**	30-10-17	Analyzing code	,,	Assignment - VII	
46	**4/7&8**	30-10-17	Instructions in Detail	,,		
47	**5/7&8**	02-11-17	Time, etc. – A more detailed look, Response Time	,,		
48	**6/7&8**	03-11-17	Time Loading	,,		
49	**7/7&8**	04-11-17	Memory Loading	,,		
50	**8/7&8**	10-11-17	Evaluating Performance, Thoughts on Performance Optimization	Board & chalk	Assignment - VIII	
51	**9/7&8**	10-11-17	Performance optimization, Tricks of the Trade	,,		
52	**10/7&8**	14-11-17	Hardware Accelerators	,,		
53	**11/7&8**	15-11-17	Caches and Performance.	,,		
54	**12/7&8**	16-11-17	Revision	,,		

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics and Communication

SEMESTER	: VII	NAME OF THE FACULT	:Abhilasha Sharma
BRANCH	: ECE "A" and "B"	DATE OF COMMENCEMENT	:17.08.2017
SUBJECT	: OPTICAL FIBER COMMUNICATION	DATE OF CLOSING	:25.11.2017
SUBJECT CODE	:10EC72	CLASS STRENGTH	:48 ,53
NO OF HRS/WK	:5	TOTAL HRS	:63

Session No	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	1/1	17-08-2017	INTRODUCTION TO THE SUBJECTS.ADVANTAGE OF OFC AND DISADVANTAGE	Board, chalk, duster		
2	2/1	18-08-2017	GENERAL COMMUNICATION SYSTEM , APPLICATION OF OFC,OPTICAL FIBER WAVEGUIDE	,,		
3	3/1	19-08-2017	RAY THEORY ,CYLINDRICAL FIBER ,SINGLE MODE FIBER	,,		
4	4/1	21-08-2017	PROBLEMS ON NUMMERICAL APERTURE & PROBLEMS ON ACCEPTANCE ANGLE	,,		
5	5/1	22-08-2017	CUTOFF WAVE LENGTH ,MODE FILED DIAMETER OPTICAL FIBERS MATERIAL	,,		
6	6/1	23-08-2017	PHOTONIC CRYSTAL FIBER OPTIC CABLES	,,		
7	7/1	24-08-2017	HALLIGENIDE AND CHALCOGENDIE FIBERS	,,		
8	1/2	28-08-2017	UNIT:-2 TRANSMISSION CHARATERISTIC OF OPTICAL FIBERS ,ATTENUATION LOSS PROBLEMS ON ATTENUATION LOSS	,,		
9	2/2	29-08-2017	ABSORPTION LOSS, EXTRINSIC AND	,,		

			INTRINCSIC			
10	3/2	30-08-2017	SCATTERING LOSS, LINEAR AND NON LINEAR SCATTERING LOSS	,,		
11	4/2	31-09-2017	BENDING LOSS, PROBLEMS ON RAYLEIGH RAMAN SCATTERING	,,		
12	5/2	01-09-2017	DISERSION , INTRAMODAL AND INTERMODAL DISPERSION	,,		
13	6/2	04-09-2017	TEST ON LINEAR AND NON LINEAR SCATTERING	,,		
14	1/3	05-09-2017	OPTICAL SOURCES , THEORY FOR OPTICAL OPTICAL SOURCE INTRODUCTION	,,		
15	2/3	06-09-2017	LED, LASER DIODES, POPULATION INVERSION	,,		
16	3/3	07-09-2017	PHOTO DETECTORS , QUANTUM EFFICENCY	,,	A1	
17	4/3	08-09-2017	RESPONSE TIME, PROBLEMS ON RESPONSE TIME	,,		
18	5/3	09-09-2017	PHOTO DETECTOR NOISE, DOUBLE HETRO JUNCTION STURCTURE FOR LED	,,		
19	6/3	11-09-2017	PHOTO DIODES , DOUBLE HETRO JUNCTION FOR LASER	,,		
20	7/3	12-09-2017	COMPARIOSN OF PHOTO DETECTORS UNIT 3:- FIBER COUPLERS	,,		
21	1/4	13-09-2017	FIBER COUPLERS, CONNECTORS SPLICES,	,,		
22	2/4	14-09-2017	FIBER MISALGNMENT AND JOINT LOSS	,,		
23	3/4	15-09-2017	SINGLE MODE FIBER JOINTS	,,		
24	4/4	22-09-2017	FIBER SPLICES	,,		
25	5/4	23-09-2017	FIBER CONNECTORS ,FIBER COUPLERS	,,		

26	1/5	25-09-2017	OPICAL RECEIVER ,INTRODUCTION	,,		
27	2/5	26-09-2017	OPICAL RECEIVER OPERATION	,,		
28	3/5	27-09-2017	RECEIVER SENSTIVITY	,,		
29	4/5	28-09-2017	QUANTUM LIMIT,EYE DIAGRAM	,,		
30	5/5	03-10-2017	COHERENT DETECTION	,,	A4	
31	6/5	04-10-2017	BURST MODE RECEIVER , OPERATION ANALOG RECEIVER	,,		
32	1/6	09-10-2017	ANALOG AND DIGITAL LINKS INTRODUCTION	,,		
33	2/6	06-10-2017	OVERIVIEW OF ANALOG LINKS ,CNR	,,		
34	3/6	07-10-2017	MULTICHANNEL TRANSMISSION TECHNIQUE,RF OVER FIBER	,,		
35	4/6	09-10-2017	KEY LINK PARAMETERS, RADIO OVER FIBER LINKS	,,		
36	5/6	10-10-2017	RADIO OVER FIBER LINKS ,MICROWAVE PHOTONICS	,,		
37	6/6	11-10-2017	DIGITAL LINKS:-POINT TO POINT LINKS	,,		
38	7/6	12-10-2017	SYSTEM CONSIDERATION , LINK POWER BUDGET	,,		
39	8/6	13-10-2017	SHORT WAVE LENGTH BAND, TRANSMISSION DISTANCE FOR SINGLE MODE	,,		
40	9/6	14-10-2017	POWER PENALTIES, NODAL NOISE	,,		
41	10/6	16-10-2017	NODAL NOISE AND CHIRPING	,,	A2	

42	1/7	17-10-2017	WDM CONCEPTS AND COMPONETS	,,		
43	2/7	26-10-2017	OVERVIEW OF WDM OPERATION PRINCIPLES WDM STANDARDS	,,		
44	3/7	27-10-2017	MACH-ZEHENDER INTERFEROMETER, MULTIPLEXER	,,		
45	4/7	28-10-2017	MEMS TECHNOLOGY, VARIABLE OPTICAL ATTEUNATOR	,,		
46	5/7	30-10-2017	TUNABLE OPTICAL FIBER, DYNAMIC GAIN EQUALIZER	,,		
47	6/7	31-10-2017	OPTICAL DROP MULTIPLEXER POLARIZATION CONTROLLER	,,		
48	7/7	2-11-2017	CHROMATIC DISPERSION COMPENSATOR TUNABLE LIGHT SOURCES	,,		
49	8/7	3-11-2017	TEST ON CHAPTER 7	,,		
50	1/8	4-11-2017	OPTICAL AMPLIFIER AND NETWORKS	,,		
51	2/8	9-11-2017	OPTICAL AMPLIFIER	,,	A6	
52	3/8	10-11-2017	BASIC APPLICATIONS AND TYPES	,,		
53	4/8	13-11-2017	SEMICONDUCTOR OPTICAL AMPLIFIER	,,		
54	5/8	14-11-2017	OPTICAL NETWROKS ,INTRODUCTION	,,	A7	
55	6/8	15-11-2017	SONET /SDH, OPTICAL INTERFACES	,,		
56	7/8	16-11-2017	SONET /SDH RINGS, HIGH SPEED ,LIGHT WAVEGUIDES	,,		

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CMR INSTITUTE OF TECHNOLOGY

Session wise – Course Plan

Department of Electronics & Communication Engineering

SEMESTER : VII
NAME OF THE FACULTY : Tania H M
BRANCH : ECE
DATE OF COMMENCEMENT : 19/08/2017
SUBJECT : Power Electronics
DATE OF CLOSING : 5/11/2017
SUBJECT CODE : 10EC73
CLASS STRENGTH : 55/53
NO OF HRS/WK : 5
TOTAL HRS : 57

Session	Chapter no (No of hrs planed for the chapter)	DATE	Topics planned for the session	Teaching Aids	Assignments/ Tests planned for the chapter	Topics covered As per plan
1	**1/1**	19/08/2017	Applications of Power Electronics,			
2	**1/2**	21/08/2017	Peripheral Effects, Characteristics and Specifications of Switches.			
3	**1/3**	22/08/2017	Diode Characteristics, Reverse Recovery Characteristics		Assignment 1	
4	**1/4**	23/08/2017	Power Diode Types, Silicon Carbide Diodes			
5	**1/5**	24/08/2017	Power semiconductor devices, Control characteristics			
6	**1/6**	28/08/2017	Peripheral effects			
7	**1/7**	29/08/2017	Types of Power Electronic Circuits			
8	**1/8**	30/08/2017	Introduction to SCR			
9	**1/9**	31/08/2017	Introduction to SCR			
10	**2/1**	01/09/2017	Introduction, Power MOSFETs – Steady State Characteristics**.**			
11	**2/2**	04/09/2017	Switching Characteristics			

12	**2/3**	05/09/2017	Bipolar Junction Transistors – Steady State Characteristics			
13	**2/4**	06/09/2017	Switching Characteristics, Switching Limits		Assignment 2	
14	**2/5**	07/09/2017	IGBTs, MOSFET Gate Drive			
	2/6	08/09/2017	BJT Base Drive, Isolation of Gate and Base Drives			
15	**2/7**	09/09/2017	Pulse transformers			
16	**2/8**	11/09/2017	Opto-couplers			
17	**3/1**	12/09/2017	Introduction, Thyristor Characteristics			
18	**3/2**	13/09/2017	Two-Transistor Model of Thyristor			
19	**3/3**	14/09/2017	Thyristor Turn- On, Thyristor Turn-Off			
20	**3/4**	15/09/2017	A brief study on Thyristor Types			
21	**3/5**	22/09/2017	Series Operation of Thyristors, Parallel Operation of Thyristors			
22	**3/6**	23/09/2017	*di/dt*Protection, *dv/dt*Protection			
23	**3/7**	25/09/2017	DIAC, Thyristor Firing Circuits, Unijunction Transistor			
24	**4/1**	26/09/2017	Introduction			
25	**4/2**	03/10/2017	Principles of phase controlled converter operation,		Assignment 3	
26	**4/3**	04/10/2017	Dual converters			
27	**4/4**	06/10/2017	1φ fully controlled converters,			
28	**4/5**	07/10/2017	1 φ semi converters (all converters with R & RL load			
29	**4/6**	09/10/2017	Numericals			
30	**4/7**	10/10/2017	Numericals			
31	**4/8**	11/10/2017	Numericals			
32	**5/1**	12/10/2017	Thyristor turn off methods, , external pulse commutation.			
33	**5/2**	13/10/2017	self commutation			
34	**5/3**	14/10/2017	class A and class B types			

35	**5/4**	16/10/2017	Complementary commutation,			
36	**5/5**	17/10/2017	auxiliary commutation,			
37	**5/6**	23/10/2017	natural and forced commutation, AC line commutation, numerical problems			
38	**6/1**	24/10/2017	**AC Voltage Controllers:** Introduction			
39	**6/2**	25/10/2017	Single-Phase Full-Wave Controllers with Resistive Loads		Assignment 4	
40	**6/3**	26/10/2017	Single- Phase Full-Wave Controllers with Inductive Loads			
41	**6/4**	27/10/2017	Numericals			
42	**6/5**	28/10/2017	Numericals			
43	**6/6**	30/10/2017	Numericals			
44	**7/1**	31/10/2017	**DC-DC Converters:** Introduction			
45	**7/2**	02/11/2017	Principle of step down and step up chopper with RL load			
46	**7/3**	03/11/2017	Performance parameters		Assignment 5	
47	**7/4**	04/11/2017	DC-DC converter classification			
48	**7/5**	05/11/2017	Numericals			
49	**7/6**	8/11/2017	Numericals			
50	**8/1**	10/11/2017	**DC-AC converters**: Introduction			
51	**8/2**	11/11/2017	Principle of operation single phase bridge inverters			
52	**8/3**	12/11/2017	Three phase bridge inverters			
53	**8/4**	13/11/2017	Voltage control of single phase inverters, Harmonic reductions			
54		14/11/2017	Revision			
55		15/11/2017	Revision			
56		16/11/2017				
57		17/11/2017				

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